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ADAPTING TO FASTER PACED DEVELOPMENT CYCLES WITH ADAPTATION LAYERS - PAGE 32

IDEAS
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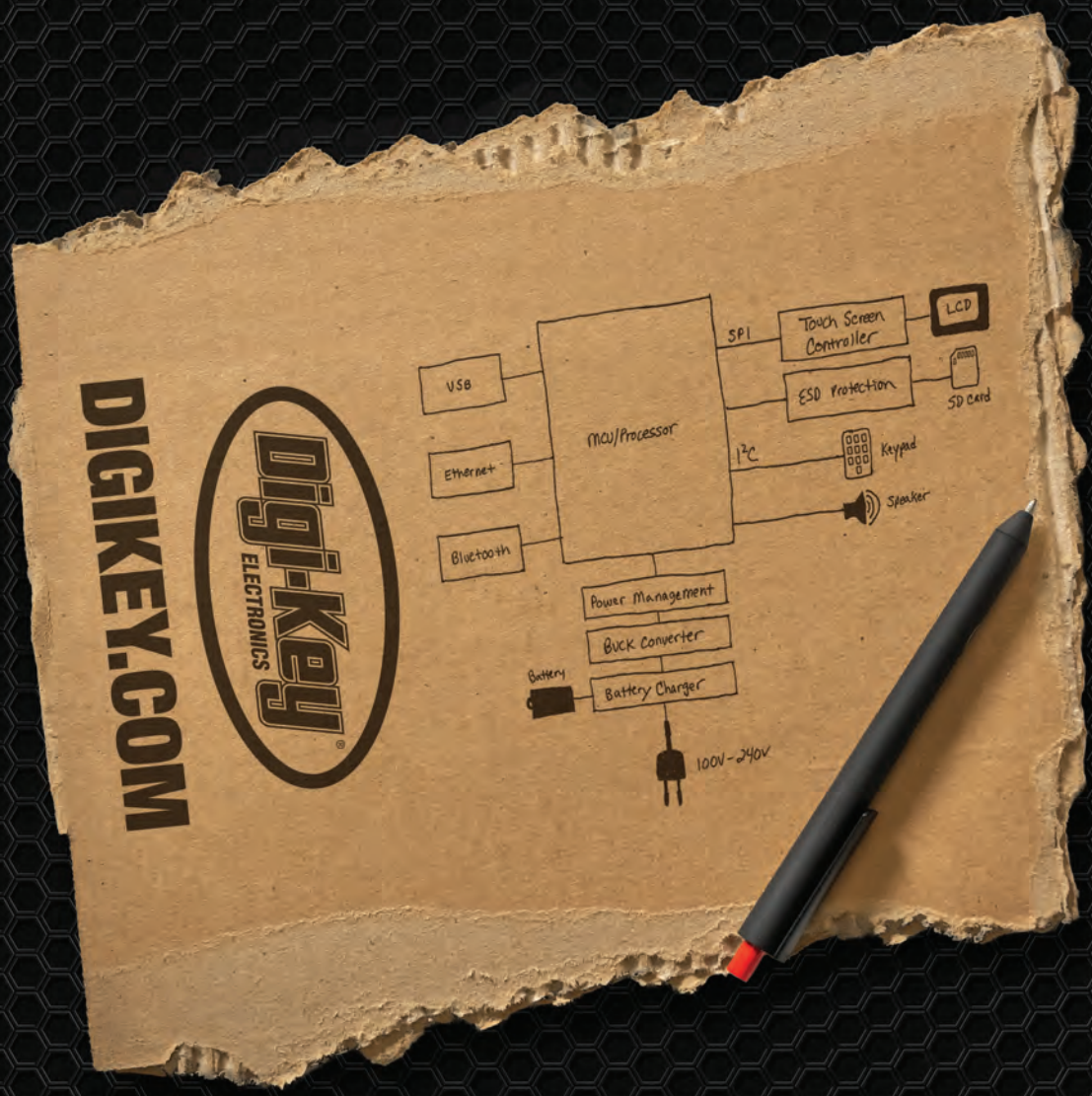

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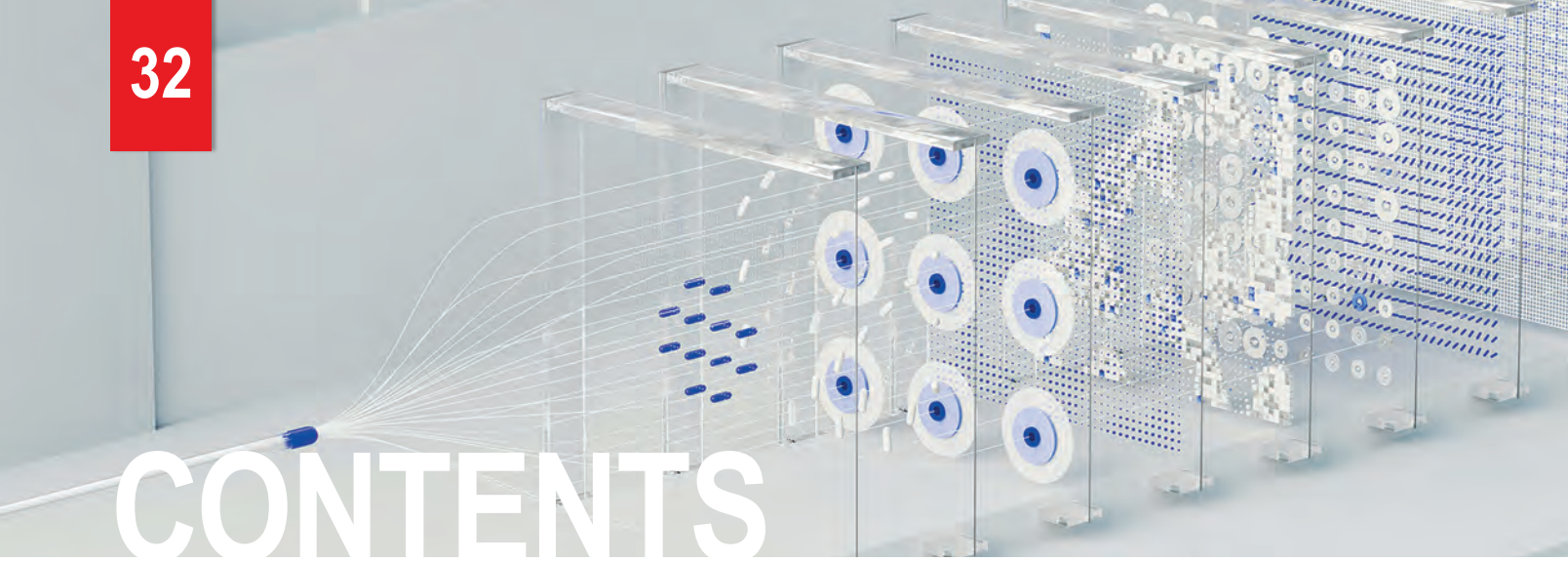

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EDITORS WORD

That's nuts!

It's easy to become so enamored with your own discipline that you blinker yourself to things going on around you. However, although the "nothing to do with me" approach may be easy, it's not a great idea.

I remember deep in the mists of time we used to call the 1980s when the company I was with developed a UNIX accelerator. This was about the size of a small filing cabinet. It sat next to the main UNIX computer and speeded the processing of heavy-duty applications by one or two orders of magnitude. I was focused on the digital portion of the design, so the enclosure fell into the "nothing to do with me" category.

The final step was to send our creation off to a special vibration testing facility. It failed. We were sad. The laboratory reported that, by the time our unit arrived with them to be tested, the nuts holding its cooling fan had vibrated off their machine screws and the fan ended up in the guts of the processing engine.

I only wish I'd been aware of a special type of fixture called a Nord-Lock washer that I discovered just yesterday as I pen these words (bit.ly/3mbIzAS).

That's the great thing about DENA. It's a one-stop-shop where you can dip your toes into other disciplines' waters. In this issue, for example, hardware designers can learn about MISRA C (Page 12), while software developers can acquaint themselves with power supplies (Page 40). Stay curious my friends!

Max Maxfield

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Editor, DENA

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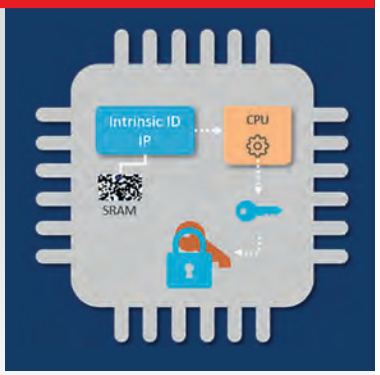
TOP STORY

Intrinsic ID announces post-quantum security solution

Intrinsic ID is well known for its SRAM-based physically unclonable function (PUF) technology. Due to tiny process variations in the silicon, many of the SRAM cells will always power up containing the same 0 or 1 values (others will vary, but that's not important). Intrinsic ID employs this feature to generate unique device IDs and cryptographic keys.

Previously, Intrinsic ID's technology has been presented as hardware IP that has to be built into the silicon. Now, the company has released its Zign X00 series of software products, which can be deployed in any digital device that offers processing capabilities (MCUs, FPGAs, SoCs, etc.), including existing chips that are already on the shelves or in the field. As reported on EEJournal.com, *Yes! On-Chip Generation of Post-Quantum Secure IDs and Keys* **(https://bit.ly/3GzpAHo)**, all that is required is for a small amount (1KB) of the SRAM that's already inside the device to be reserved for use as that device's PUF, while all of the other functions are realized in software code rather than hardware logic gates. The software is provided in the form of a compiled library with associated API for use with any standard processor core (Arm, ARC, MIPS, RISC-V, X86, Xtensa, etc.).



www.intrinsic-id.com

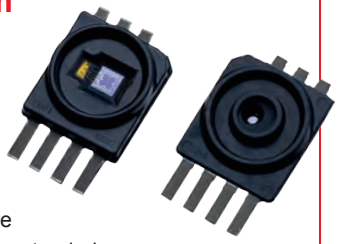
Keystone introduces new slide-in PCB mount battery contacts

To meet increasing demands for higher energy, lower weight cylindrical battery usage, Keystone Electronics has introduced its latest leaf spring contacts designed to slide into molded cases with wire leads or mounted directly onto a PCB as a surface-mount contact.

Engineered with a contact design that adjusts to variations in battery length, these contacts ensure low contact resistance and dependable connectivity. Manufactured from 0.012" (0.30mm) thick spring steel and supplied with nickel plating for superior performance in today's high-tech devices, contacts are designed to accommodate A, AA, and CR2 cylindrical batteries.

www.keyelco.com

Melexis releases PCB-less pressure sensor IC platform



Melexis has added two new products to its family of PCB-less pressure sensors with extended robustness to harsh environments and media. The MLX90823 (analog output) and MLX90825 (digital SENT output) are relative pressure sensors that can be used in gauge mode (vs. atmospheric pressure) or in differential mode (with two variable pressure levels). Unlike absolute pressure sensors, they measure the pressure difference between the two sides of the sensor.

In the case of automotive applications, for example, access to stable and accurate data on pressure and temperature facilitates full lifetime engine management. These factory-calibrated devices, which are intended to measure pressures spanning 0.1 to 1.5 bar, demonstrate a combination of accuracy and performance not previously seen in the automotive industry.

www.melexis.com

DIGISTOR's FIPS 140-2 L2 SSDs added to CSfC component list

DIGISTOR, a leading provider of secure data-at-rest (DAR) storage solutions, announced that the National Security Administration (NSA) added its FIPS 140-2 L2 SSDs to the Commercial Solutions for Classified (CSfC) list.

CSfC is an NSA strategy to provide cybersecurity solutions by taking advantage of commercially available industry solutions. With the CSfC listing, customers can trust that the solutions they develop for securing DAR in laptops, desktops, and other devices, meet the highest security requirements for sensitive and classified data. DIGISTOR FIPS 140-2 L2 drives are the only commercial SSDs to achieve this listing, making the company's Citadel K Series the simplest and most affordable way to produce CSfC-level secure data-at-rest (DAR) solutions for top secret programs.

www.digistor.com

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With the new optocouplers, Würth Elektronik presents one of the latest additions to its optoelectronic product portfolio. The innovative design features a coplanar structure and high-grade silicon for total internal reflection. The coplanar design ensures the isolation gap stay fixed during the production process and provide perfect isolation and protection for your application. The total internal reflection provide stable CTR over the whole temperature range and high CTR even at low current operation.

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Highlights

- Innovative coplanar design
- High grade silicon encapsulation
- Copper leadframe for high reliability
- Stable CTR over whole temperature range
- High CTR in low current operation

DIP-4 SOP-4 LSOP-4

OKW offers fluorescent and photoluminescent printing

Attracting attention is desirable in diffuse lighting conditions and critical in hazardous areas, so OKW has expanded its range of custom printing colors to meet these requirements.

Customers can now specify OKW's products with labels and graphics produced (by screen or tampo printing) using new fluorescent inks, which are ideal for warning messages or for attracting attention to equipment such as emergency electronics.

It is also often important to consider the visibility of safety and orientation signs, or the highlighting of specific device functions during hours of darkness or in low light levels. For this purpose, OKW now offers photoluminescent (phosphorescent) inks.

www.okwenclosures.com

Microchip unveils MPLAB SiC power simulator

The electrification of everything is driving the growth of silicon carbide (SiC) semiconductors. Large market segments such as E-Mobility, sustainability, and industry are turning to SiC-based power solutions because of SiC's fast-switching capabilities, lower power loss, and higher temperature performance.

To help design engineers transition to SiC power solutions with ease, speed, and confidence, Microchip has announced its MPLAB SiC Power Simulator, which can be used to quickly evaluate Microchip's SiC power devices and modules across various topologies before committing a design to hardware. The tool can speed up time to market by delivering a comprehensive SiC evaluation that not only provides valuable benchmarking data but also reduces component selection times.

www.microchip.com

Arduino introduces Portenta C33 SOM

Arduino has announced the launch of its new Portenta C33 system-on-module (SOM), which is based on the RA6M5, an Arm Cortex M33-based microcontroller from Renesas. The C33 is the latest addition to Arduino's Portenta family, which is specifically designed to provide a complete and scalable platform for IoT edge devices. The Portenta C33 offers a powerful microcontroller, connectivity, and security at a convenient price point, making it ideal for a vast range of applications, such as Edge AI devices, IoT gateways, remote control systems, fleet management, and process tracking.

The Portenta C33 provides professional developers with a production ready IoT platform combining the familiar Arduino environment with other high-level languages like MicroPython. The module integrates Wi-Fi and Bluetooth Low Energy connectivity alongside a wide variety of peripheral interfaces, including CAN, SAI, SPI and I2C. Furthermore, the RA6M5's integrated Secure Crypto Engine 9 (SCE9) with secure key storage ensures industrial-grade security at the hardware level and the ability to perform over-the-air firmware updates with Arduino IoT Cloud or other third-party services.

www.arduino.cc/pro

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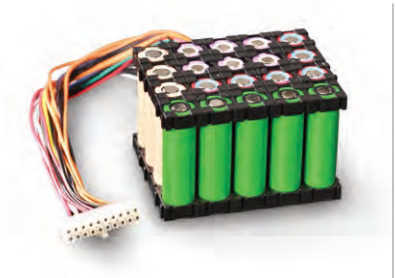

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Reducing safety and security risks for embedded systems

Bill Lamie, President & CEO, PX5 RTOS

Introducing a new mechanism to detect and mitigate memory corruption in MCU-based applications

Embedded software developers working at the real-time operating system (RTOS) level know that memory corruption issues are easy to introduce, difficult to detect, and often devasting to application safety and security. This makes preventing these issues a popular subject among providers of industry standards, test tools, and RTOS solutions. Despite this, there remain significant constraints in mitigating memory corruption on microcontroller unit (MCU) devices as they are unable to support the more sophisticated programming and RTOS techniques.

At the core of billions of applications worldwide, MCUs present unique safety and security challenges. With no memory management unit (MMU) or memory protection unit (MPU), and with little capacity for including memory protection features in code, MCUs provide embedded developers few options for ensuring the robustness of their systems.

As MCU deployments continue to rise and support more connected systems, developers need better methods to protect against memory corruption issues without compromising the strict functional and performance requirements of these hard real-time systems.

Challenges in safety and security for MCU-based applications

To minimize processor workloads and memory footprints, MCU-based applications tend to run within a single address space that is shared globally across all threads. Unlike applications running on a higher-level RTOS—such as Embedded Linux—that partitions memory into different address spaces, MCU applications have access to the entire range of memory. This monolithic approach puts the burden on developers to find their own ways of preventing application functions from corrupting memory outside their own segments.

Corruption occurs when data inside a memory location is changed through unexpected or undesirable means, such as the alteration of a pointer from a valid to suspicious address. For example, the corruption of function pointers could lead to program execution jumping to an invalid memory location, causing a system failure. If hackers suspect this weakness exists, they can exploit the unprotected pointer to misdirect execution to malicious code they have introduced through a technique called code injection.

Protecting against memory corruption requires both foresight and knowledge. Developers need to recognize when an issue may occur (not always easy in applications with multiple threads accessing the same memory locations) and know how to minimize its probability

Continues on page 10 >

Table 1: Memory allocations for function pointer verification example (Source: PX5 RTOS)

Memory	Symbol	Address	Notes
FLASH	start_routine()	0x2376D	The application's start routine
RAM	px5_thread_control	0x200001A0	The PX5 RTOS control structure containing the function pointer to start_routine() and other thread information
	entry_routine	0x20000204	The structure member where the start_routine() function pointer is saved
	entry_routine_verification_code	0x20000208	The structure member where the PDV verification code for the entry_routine function pointer is stored

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of occurrence. Here are some typical remediation strategies for devices without built-in memory protection:

• NULL pointer checks to ensure references are pointing to valid memory locations when used.
• Using checksums or CRC to detect and handle potentially unsafe memory accesses.
• Comparing values to data stored in different memory locations to see if they match.

These techniques consume device resources and rely on the developer remembering where to use them. The latter two also require considerable effort in planning, architecture, and testing.

The PX5 RTOS, designed for demanding MCU-based applications, offers a built-in approach to memory protection that minimizes developer and device overhead. This approach is called Pointer Data Verification (PDV).

Mitigating memory corruption with PDV

PDV is a lean and robust method of memory address verification unique to the PX5 RTOS. Designed specifically for resource-constrained MCU applications that lack access to an MMU or MPU, PDV is a software-only technique that creates and stores a unique verification code for memory structures to help applications avoid unexpected and unauthorized accesses.

Once a developer turns on PDV, the PX5 RTOS automatically creates verification codes upon loading values to sensitive data locations. Before the application uses the sensitive data, the RTOS generates the verification code again and compares it with the stored value. If these two codes fail to match, the PX5 RTOS calls a central error handling function that executes actions specified by the developer.

Developers can define the formula for generating the verification code or use the default mechanism provided by the PX5 RTOS. The default verification code is a combination of a secret runtime identification passed to the RTOS (such as the result from a true random number generator), the value of the sensitive data, and the address to store the generated code. The default formula looks similar to this:

```
Verification Code
= ((Data Value) +
(Address to Store
Code) + (Secret))
^ (Secret)
```

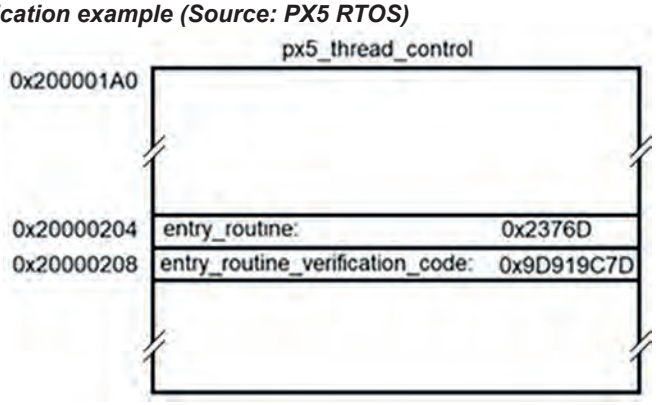
How developers use PDV

One example of how developers can use PDV to protect sensitive data structures is that of Function Pointer Verification (FPV). When building an application with the PX5 RTOS, developers can use the `PX5_FUNCTION_POINTER_VERIFY_ENABLE` flag to ensure verification of all function pointers before their use. Take this example of creating an application's start routine function pointer using the POSIX Threads (pthreads) API supported by the PX5 RTOS:

```
int pthread_create(pthread_t * thread_handle,
                   pthread_attr_t * attributes,
                   void * (* start_routine)(void *),
                   void * argument);
```

Let's say the compiler allocates memory as specified in Table 1. Let's further state that the computed verification code for the entry_routine function pointer is 0x9D919C7D. Figure 1 shows the thread control block after thread creation, both in raw memory format and as a data watch.

Figure 1: Thread control block for function pointer verification example (Source: PX5 RTOS)



When the start_routine() function pointer is used during runtime, the PX5 RTOS recalculates the verification code and compares it with the stored verification code, 0x9D919C7D. If the newly computed code matches the stored code, the function pointer is considered valid and the function start_routine() is called. If the codes fail to match, there is a high likelihood of memory corruption in either the function pointer or the stored verification code, so the PX5 RTOS calls the central error handling function.

Through this approach, a hacker attempting to remotely alter program execution would fail as their injected code is unable to generate a matching verification code.

Protecting against memory corruption from the ground up

PDV is patent-pending technology that provides developers with robust detection and mitigation of memory corruption issues without compromising application performance or resource budgets. The PX5 RTOS itself is ultra-small (less than 1 KB for minimal use), ultra-portable (with a fully compliant pthreads API), and rigorously tested (100% C statement and branch decision coverage for every release), making it the ideal foundation for systems requiring robust determinism, safety, and security.

Although PDV is designed for MCU environments without memory protection hardware, it can also supplement code safety and security practices for more robust processors having MPU and/or MMU capabilities.

www.px5rtos.com

"Developers need better methods to protect against memory corruption issues without compromising the strict functional and performance requirements of these hard real-time systems"

Everyone loves robots

The worst challenges to having the robots we want are non-technological

Let's face it, everyone loves robots. They've been indispensable as a science-fiction mainstay longer than most folks have been alive. Now, tantalizingly, is the possibility that real robots, the kind we all want, will become a reality, but there are challenges, the worst being non-technological.

In the 60s and 70s we all thought we'd be traveling to work in flying cars and living on the Moon by 2001. That didn't happen, not because those things were not technologically achievable, but because we did something else. Two generations of humans took a 40-year hiatus to build the internet, including the underlying technologies that make it all work.

Recently, hardware in the form of rockets, robots, and autonomous cars has seen a resurgence in interest as investors began to wonder if the best fruit was disappearing from the tree of software. Briefly, robots had a chance, but now there is AI. Many people imagine AI would enable robotics, but this is not the dynamic we are seeing. AI is a new software tree promising a new generation of low hanging fruit that can endow low venture investments with the possibility of dramatic returns.

For roboticists, it is on us to figure out how to make robots less costly. It is not sufficient to do exciting things—we must learn to do them cheaply enough that we can attract the capital we need to bring them to market.

A tough time is ahead for robotics. Investors will be distracted by the opportunities offered by pure-software AI companies. It is on us to re-envision robotics in a way that can evolve and grow, so we can have the robots we dream of to help make our lives better, free the world from boring labor, and—if we're lucky—lead humanity into an era of thought, imagination, and creativity.

Adrian Kaehler, AI Scientist, Roboticist, and Inventor

www.edex.ai

Why MISRA C matters

New guidance for embedded software developers

MISRA C comprises the leading guidelines that drive safe, secure, and reliable code for embedded systems from automotive to avionics to medical devices and beyond. Released in 1998, MISRA brought the C language in line with safety- and security-critical system requirements by guiding developers to avoid and eliminate potentially dangerous code.

Over the last 20 years, updated guidelines have addressed challenges encountered with C. The March 2023 release of MISRA C:2012 Amendment 4 (AMD4) and MISRA C:2023 provide the newest guidance to make MISRA more relevant than ever. These updates consolidate all previous MISRA C editions, amendments, and technical corrigenda into a single document to address the huge configuration-management challenge for developers.

Pros and cons of C for embedded development

C was originally built as a lightweight and friendlier alternative to assembler. Developer adoption rates have increased much faster than syntax or semantic updates for safety- and security-critical concerns. This poses challenges for critical applications developed using the language because it is based on standards (ISO/IEC 9899:2011 and 2018) that omit comprehensive specifications for how implementations must behave. This omission is largely by design as it gives developers greater flexibility in how they access and manage low-level system resources.

This also means developers may choose to control application behavior and memory access in unpredictable and non-deterministic ways. Such code may meet C language standard requirements but potentially cause undesirable effects in critical systems, leading to a security breach or loss of life. Examples include:

- Writing to a file stream opened as read-only leading to undesirable behavior.
- Using functions that call themselves (i.e., recursion) leading to a potential stack overflow.
- Accessing memory outside the bounds of a data structure leading to exploits by hackers.

Although some C compilers can identify multiple risky coding practices, identifying more issues before they are introduced into the code base with static analysis is far more efficient and cost-effective. Using a static analysis tool to automate MISRA C compliance can enable developers to identify and remediate issues early in the system lifecycle.

Why MISRA C matters

Since its inception, MISRA C has brought C in line with safety- and security-critical systems requirements by restricting language use to a safety-critical subset to avoid and eliminate potentially dangerous code.

MISRA C:2012 AMD4 specifically covers new concurrency features on multithreading and atomic types introduced by the C11 and C18 standards. New rules and directives restrict multithreading features to a safe subset by:

- Restricting dynamic thread creation to foster more deterministic approaches to concurrency.
- Ensuring threads are created before mutexes are linked to them.
- Minimizing risk of deadlocks and data races in the system.
- Managing safe use of thread objects and thread identifiers.

New rules and modifications support developers in their atomic pursuits by:

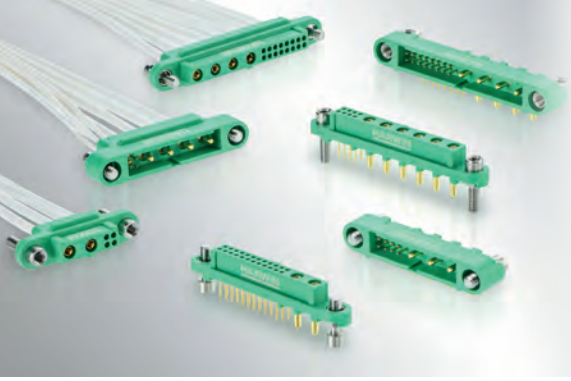
- Ensuring the correct configuration of atomic types.
- Preventing the unintended removal of atomicity when referencing atomic types through pointers.
- Restricting the use of multiple atomic types in the same statement.

Start your path toward MISRA C

MISRA C's influence cannot be overstated. It is integral to any embedded software certification process and the adoption of static analysis tools is a valuable investment toward meeting compliance goals. By advocating for these tools, developers improve the safety, security, and reliability of their code while demonstrating a commitment to higher-level business objectives.

www.ldra.com

Jay Thomas, Senior Director of Field Engineering, LDRA



Harwin increases mixed layout Hi-Rel connector portfolio

More off-the-shelf data/power contact combinations are now available for Gecko-MT

For over 70 years, Harwin has supplied engineers with the connectors needed to meet the most demanding specifications. Harwin's innovative interconnect portfolio of high-reliability products is designed for ultra-high-performance applications in the harshest operating environments or within the tightest of spaces.

Today, Harwin products are found in a wide range of markets and applications around the globe. These include space, avionics, defence, robotics, oil and gas, healthcare, motorsport, industrial drives, factory automation systems, autonomous vehicles, smart agriculture, electric vehicle battery management, and more.

Recently, Harwin expanded the contact layout options of its Gecko-MT high-reliability (Hi-Rel) connectors. Announced at Electronica in Munich, the new variants have been added to complement the existing symmetrical 2-power/8-signal and 4-power/8-signal layouts.

There are six new contact arrangements that feature 2 to 6 power contacts and 4 to 24 signal contacts. These have a non-symmetrical structure, with the power contacts situated at one end and the data contacts at the other. The power contacts have a 10A current rating, while the signal contacts are rated for 2.8A (maximum).

A range of hardware fixings are available for each contact layout. Both male and female connectors can be supplied in either standard gender or reverse fix. There are front and rear panel mount options, plus board-mount fixings to reduce any strain placed on solder joints. In total, 72 extra Gecko-MT connector variants have been added.

As with all the Gecko connectors in Harwin's HRi product offering, these latest variants have high resilience to shock and vibration, plus compact size and lightweight construction. They support a –65°C to +150°C operating temperature range, and 1,000 (minimum) mating cycle durability (evaluation samples are available on request).

All of these new Harwin Gecko-MT connectors can be rapidly shipped from stock. The company also provides a cable assembly service on all Gecko connectors, supplying ready-made, fully inspected harnesses.

www.harwin.com

Supercapacitors in robotic applications

Autonomous mobile robots and semi-autonomous cobots are candidates for supercapacitors

Commonly known as supercapacitors, electrochemical double-layer capacitors (EDLCs) are still relatively new to the electronics industry. Only recently have AEC-Q200 qualified supercapacitors entered the scene and only a few suppliers provide them. Determining their viability for a design will require research on EDLC technology, but looking at a few examples can help.

Warehouse robots, autonomous mobile robots, and semi-autonomous cobots (collaborative robots) come to mind as candidates for supercapacitor use for two main reasons: (a) they typically have a docking station for charging and (b) they frequently have tasks requiring short bursts of increased power to lift/move heavy loads.

Supercapacitors have an advantage over batteries with respect to specific power, meaning they can discharge massive amounts of current with no penalty on lifetime or reliability. They're also unlike batteries in that their charge/discharge cycles approach 1 million cycles as opposed to the thousands or possibly tens of thousands found in batteries. By comparison, if a robot needs to operate a long time remotely, batteries may offer the best solution.

An analogy that might help is the use of nitrous oxide in racing cars and drag cars for added power. At a certain distance, the weight of the nitrous (supercapacitor) would not be as efficient as having a larger gas tank (battery). We could extend this analogy to supercapacitor ESR (equivalent series resistance) contributing to the counterpart of a lower brake horsepower value. Supercapacitor modules are typically balanced with resistors, thereby adding to ESR. If the design is not too strictly weight- or size-constrained, adding a supercapacitor module to supplement the battery on peak power operations will increase efficiency and extend battery life. Similarly, for robotic applications relying on energy harvesting, supercapacitors are better suited to capturing spurious charge currents.

Another example application with implications for industrial automation robots exploiting the superior power performance of supercapacitors can be found in the kitchen. Restaurants and other non-residential buildings are charged by power companies on peak power demands. Supercapacitor banks can be used to turn on ovens, fryers, and burners during the day, while charging at night when power usage rates are lower. This leads to desirable cost savings for the business owner while also relieving strain on the grid.

PARAMETER/CHARACTERISTIC	SUPERCAPACITOR	LI-ION BATTERY
Charge Time	1To 10 Seconds	10 To 60 Minutes
Charge Cycle Life	1 Million	>500
Cell Voltage	2.1 To 3.3 Volts	3.6 To 4.2 Volts
Specific Energy (Wh/Kg)	5	100 To 200
Specific Power (W/Kg)	~10,000	1000 To 3000
Charge Temperature Range	-55°C To +90°C	0°C To +45°C
Discharge Temperature Range	-55°C To +90°C	-20°C To +60°C

Comparison of supercapacitors and Li-Ion batteries

The high current capability and high charge/discharge cycles of supercapacitors are key factors on design-in, so meeting a need for high-power demands increases viability for industrial automation.

One important point is for supercapacitor banks to be used only in environments that don't stray too far from an ambient temperature of ~25°C. A common electrolyte used in supercapacitors is acetonitrile, which begins to boil at 85°C, although there are aqueous-based systems that push this to 95°C. Of course, the best design practice to stay as far beneath the maximum temperature rating of a component as possible and this is especially so for supercapacitors. A good rule of thumb for operating temperatures is that every 10°C below the maximum rated value will double the expected lifetime of the component.

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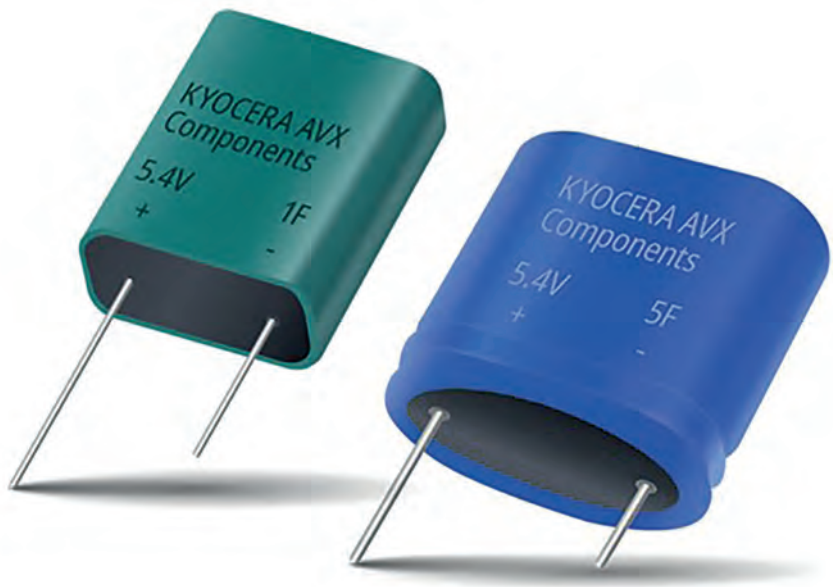

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SoC verification is no longer a one-dimensional game

New tools are required to verify SoCs with 100+ billion transistors

As technology nodes shrink, the number of transistors on chips continues to grow at an exponential rate. For example, Apple's M1 Ultra GPU with 64 cores packs in a whopping 114 billion transistors, which is 100 times more than a decade ago with the Apple A7 core.

With advancements in SerDes, computer architectures (ARM, RISC-V, X86), memory, and network-on-chip (NoC) interconnect, along with artificial intelligence/machine learning (AI/ML) algorithms, the possibilities afforded by today's system solutions implemented as system-on-chip (SoC) devices are far beyond those offered by SoCs built only ten years ago. As part of this, performance and power requirements are more aggressive than in the past, further adding to architectural and design complexity.

How about verification? Has it scaled the same way as design? The languages employed for verification have evolved from hardware/structural-oriented hardware description languages (HDLs) like VHDL and Verilog to aspect/object-oriented languages like UVM, SystemVerilog, and SystemC/C++. Meanwhile, verification platforms evolved from exclusively software simulation to a combination of simulation and formal verification along with hardware accelerated verification (HAV), which includes emulation and FPGA prototyping. Given the rapid increase in design size and complexity, verification can no longer be a "one size fits all" approach.

HDL simulation still forms the crux of IP, subsystem, and even full SoC verification provided the design is small. Another aspect of verification is co-simulation, which means running embedded software code. In this case, verification engineers need to act like firmware developers and write pseudo firmware either in C or C++ to verify the design along with a conventional UVM testbench. Although these simulations are slow, they must be performed before tape-out.

The term "shift left" refers to the practice of moving things like performance evaluation and verification as early as possible in the development process. Achieving a shift left in SoC verification is achieved by employing HAV in the form of emulation and/or FPGA prototypes to create virtual versions of the design under test (DUT). These environments allow real-world software workloads and industry benchmarks to be run prior to silicon availability, thereby enabling more testing, which increases the quality of the design. In the not-so-distant past, installing, integrating, and managing these platforms required a large team. More recently, new tools and flows and simplified integration have greatly facilitated the adoption of these techniques.

All of these HAV platforms have issues, including modelling and integrating analog modules, and synthesizing and mapping the design into the emulator/FPGA prototype. Despite these challenges, HAV is the only way to go for today's high-capacity, high-performance SoCs because it allows firmware and software development earlier in the development cycle, including elements that are critical to the tape-out of the design, such as Boot ROM code validation.

Verification has evolved over the years, albeit at a slower pace than design. The latest and greatest verification environments take full advantage of developments like Portable Stimulus, which allows the same stimulus to be used across all platforms, advances in formal algorithms to converge on evaluating different paths in the design sooner, advancements in simulators using AI algorithms to generate random stimulus based upon coverage output, running simulations in the cloud using virtual licenses for verification IPs (VIPs) on an "as-needed" basis, and several others. As a result of all this, SoC verification is no longer a one-dimensional game.

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Karthik Krishnamoorthy, Senior Manager at Micron Technology

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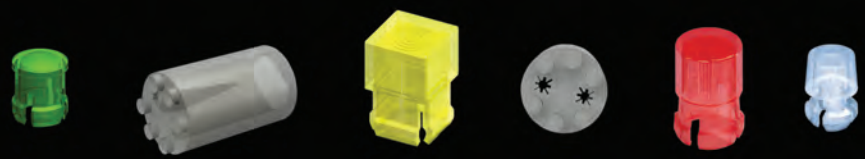
The first commercial ice-making machine was invented in 1854. In 1913, refrigerators for home use were invented and in 1923 Frigidaire introduced the first self-contained unit.

Refrigerator and freezer technologies have progressed far beyond just cold storage. Today's smart fridge and freezer units feature water & ice dispensers, user control panels & displays, Wi-Fi connectivity, voice recognition & control, and more.



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Ultrathin laptops sound off

How to get "big" audio from small speakers in ultrathin laptops

Nick Skinner, head of PC product marketing, Cirrus Logic

The workplace environment continues to see unexpected and ongoing changes in how people use their laptops. Hybrid working has elevated the importance of audio during laptop conference calls, especially in noisy environments. These changes in worker environments require an easy-to-transport laptop with a great audio experience free from headphones and external speakers.

Hybrid working environments are accelerating the adoption of ultrathin laptops, with some approaching 10-15mm—the same thickness as mobile phones. This move to slimmer, lighter laptops, along with the rise of novel laptop form factors such as 360s, detachable 2-in-1s, and folios, means that acoustic challenges are also becoming more complex.

As PC manufacturers introduce new multi-speaker laptops that are thinner than ever, smart amplifiers are at the center of smart designs that are driving and resolving these audio engineering challenges.

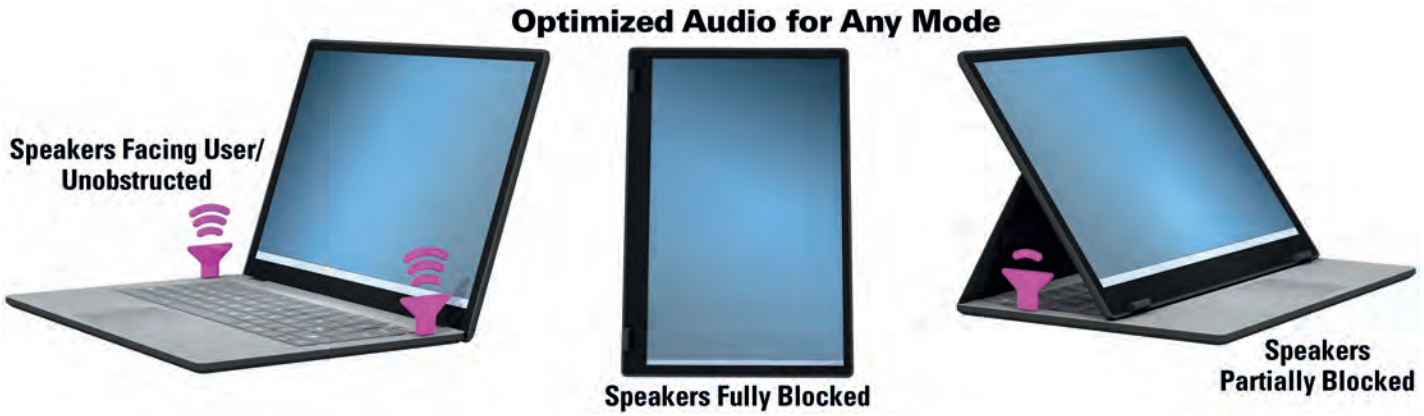
Laptop-speaker audio design challenges

Today's ultrathin laptops are used in a variety of ways and conditions that demand consistent high-quality audio. This means that the speakers inside these ultrathin notebooks must get smaller and thinner. However, the limits of physics make it difficult to get loud sound and bass from these micro speakers. In all situations, the audio should also be consistent. However, constantly shifting positions and changing environments can present challenges that dramatically impact the laptop's audio consistency.

For instance, users may choose to listen to 2-in-1s in tablet mode, tent mode, or laptop mode. In addition, low battery charge can cause conditions that limit audio loudness. Other use cases that impact the consistency of the laptop's sound quality include different volume levels and the type of audio content, such as voice, movies, music, and games. Lastly, the audio quality should hold up over time without noticeable speaker degradation or failures. Each of these use cases has different acoustic and electrical challenges.

The demand for great speaker audio is spurring OEMs to turn to smart amplifiers as the go-to technology. Smart amplifier technology extracts the best audio performance from the laptop's acoustically

Cirrus Logic enables fine-tuning for each mode and accommodates varying acoustics, ensuring consistently loud and high-quality audio for laptop, tablet, and tent mode use cases



challenging design. To achieve high-quality audio output signals, laptop designs must have full bass, low distortion, balanced sound, and limited rattle and vibration. A smart amplifier combines hardware and software to maximize loudness, quality, and consistency while minimizing rattle and protecting speakers from damage.

However, driving a speaker to maximum loudness is a delicate balance. If driven too far, the speaker will distort or even suffer permanent damage. Cranking up the volume can also cause the speakers, keyboard, chassis, and other components to rattle. The user hears this rattle as distortion and can feel unwanted vibrations. In the worst cases, the manufacturer prevents rattling by turning down the volume, compromising the audio greatness, loudness, quality, and consistency, and thus reducing the overall movie or gaming experience.

The big challenge is to make a single ultrathin laptop sound good under different uses and conditions. The audio signals must sound consistent for different content types, such as voice, music, and games, and at different volumes and battery levels. The audio quality should also be consistent over time for these devices, without noticeable speaker degradation or failures.

DSP smart amplifiers optimize PC audio

Smart amplifiers solve these challenges by combining an amplifier with an integrated digital signal processor (DSP) that runs intelligent algorithms with speaker physics models to maximize speaker performance and consistency. This processor, combined with the speaker sensing hardware, allows the amplifier to push the speaker further while—at the same time—protecting it from damage. Compared to basic amplifiers, smart amplifiers can achieve 2X or more sound pressure level (SPL).

In addition, OEMs combat loudness limitations in ultrathin laptops by using new cutting-edge speaker types designed to extract better audio. These include high-excursion and dual force-cancelling speakers, which need smart amplifiers with high drive strength to execute maximum performance. For example, high-excursion speakers require a powerful, high-voltage smart amplifier to achieve louder audio and higher dynamic range, while new dual force-cancelling speakers rely on powerful, high-drive strength smart amplifiers to provide a listening experience with low rattle, low distortion, high dynamic range, and bass loudness.

Enhancement algorithms maintain high-quality audio

Everyone's definition of audio quality differs. Generally, however, universal care-abouts include loudness, low distortion, balanced response, transparency, and less rattle. Smart amplifiers help drive micro speakers to their limits in the bass regions and, in many cases, extend the frequency range for deeper bass. A balanced or "flat" response is possible when no single frequency range, such as low, middle or high, is dominant.

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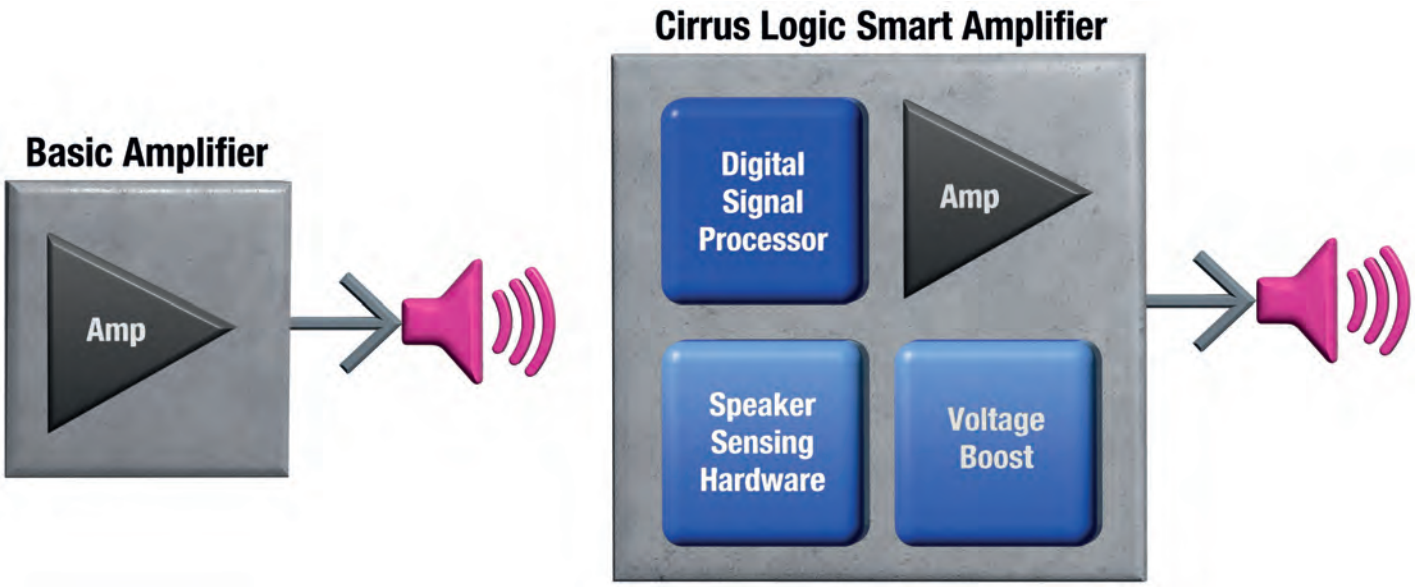

High-quality audio requires smart amplifiers with high drive strengths for maximum audio loudness and performance

Implementing this strategy through on-chip algorithms makes for a more pleasant sound.

Low distortion helps clarity and intelligibility, especially for voice calls. Enhancement algorithms help balance the speaker's response by measuring that response in order to cancel out any unwanted peaks or valleys.

Rattle is a dynamic and tricky audio problem. Certain content like ring tones and human voices may excite audible rattle, while other content like pop music may not trigger such an effect. When the speaker vibrates, it can cause a knock-on effect where other parts of the system, like the keyboard or chassis, will also rattle. This unwanted vibration can create a bad user experience, and the user may even perceive the vibration as audio distortion, which degrades clarity and intelligibility.

Cirrus Logic smart amplifiers with on-board signal processing can enable higher quality with enhancement algorithms. For example, a dynamic bass extension algorithm maximizes bass loudness and depth for any volume level. A fast-tuning change feature optimizes sound quality for each different deployment mode, such as tablet, tent, or laptop modes. Finally, a battery management algorithm adjusts tuning as battery voltage falls to maximize loudness and minimize distortion.

Support for the MIPI SoundWire interface

At the same time as laptops are getting thinner, the industry is transitioning to a new SoundWire interface for simple integration with a SoundWire Device Class Audio (SDCA) host. SDCA will make the integration of audio components simpler by providing a common way to describe audio components of the same class with reduced software overhead and complexity.

The SoundWire interface helps developers add intelligence to audio devices without unnecessary software complexity, thereby allowing these products to be brought to the market faster and at lower cost. Designing in a smart amplifier with software capabilities to support this change will ease the transition for OEMs and enable them to deliver a better user experience.

Smart amplifiers propel laptop audio

With current mobility and remote working requirements, laptop audio has become part of our personal and business lives. Dramatically reducing laptop sizes to ultrathin, lightweight, and flexible form factors complicates the audio challenges associated with remote and mobile user environments.

The newest most innovative laptops use smart amplifiers to extract the fullest design benefits, giving consumers a great audio experience with big sound. Smart amplifiers, executed with advanced algorithms, deliver superior audio quality through multiple speakers to produce an immersive audio experience for movies, music, games, and voice despite today's demanding mobile user environment.

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"Dramatically reducing laptop sizes to ultrathin, lightweight, and flexible form factors complicates the audio challenges associated with remote and mobile user environments"

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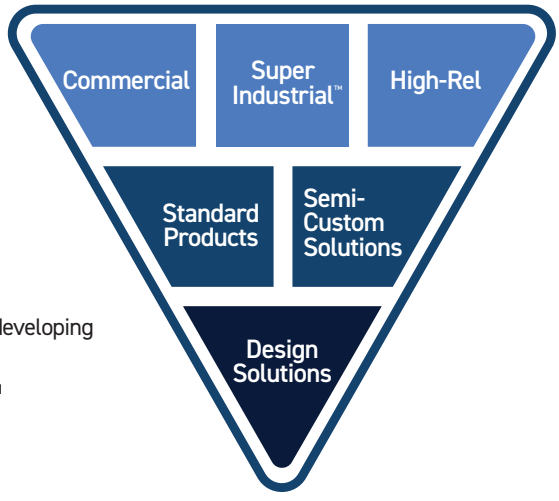

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Demystifying AI use in the electronics design chain

Generative artificial intelligence has entered the design engineering workplace. How will engineers use it and how will it impact the future of the profession?

Hate or love it, generative artificial intelligence (AI) has entered the global electronics design chain lexicon, as it has all sectors of the economy. How design engineers are using products such as ChatGPT and the multiple variants unveiled recently, though, remains unclear many months after it took the world by storm late in 2022.

Design engineers contributed to the development of AI and fostered its use with their innovations in semiconductors, communication, data and networking and cloud services but they are themselves only just discovering and exploring the potentials of AI in their professional activities, according to industry observers. Generative AI, they said, will play a significant role in future design activities but the extent to which engineers will rely on it at various points in the design cycle is still unknown. All segments of the economy are facing the same challenge, said Paul Daugherty, group CEO and CTO at Accenture.

"This technology is set to fundamentally transform everything from science, to business, to healthcare, for instance, to society itself," Daugherty said, in a recent research paper co-authored with other Accenture analysts. "Embedded into the enterprise digital core, generative AI and foundation models will optimize tasks, augment human capabilities, and open up new avenues for growth. In the process, these technologies will create an entirely new language for enterprise reinvention. But reimagining how work gets done, and helping people keep up with technology-driven change, will be essential in realizing the full potential."

The technology innovators who fostered and advanced the creation of generative AI are only now beginning to confront the knotty riddle of its existence and future. For some, the mystery of generative AI has been slowly unwinding while many others have taken a wait-and-see attitude, analysts said. They want to first understand how generative AI design solutions will compliment traditional design methodologies, said Swiss engineering consulting firm Neural Concept. What generative AI will immediately unleash is a torrent of simulations that can help cut down on the design cycle, the company said, in a position paper on what it termed "generative AI design."

"By coupling design and simulation, generative design can optimize a design for specific performance criteria – such as strength, weight, and cost – leading to improved final product performance," Neural Concept noted. "Engineers can utilize generative design to optimize existing designs to reduce weight, increase performance, or lower production costs, thus giving their companies a competitive edge."

That is only the beginning. "Generative design has the potential to revolutionize the way we design products and manufacture them because it enables designers and engineers to explore a much more extensive range of design options and find optimal solutions," the company added. How this process will work, though, is still being explored by enterprises, which must proceed slowly and with caution to avoid overwhelming engineers or tipping off competitors to products under development.

Going first or last?

Which generation of engineers will gravitate quickly to generative AI is another unknown. The younger generation may see AI as a natural extension of the digital products they grew up using. Familiarity with online products to supplement design activities may not translate into faster adoption, though, according to observers.

Veteran electronics design engineers may distrust ChatGPT, they noted. This group may even disdain and mock GPT-4 – the latest variant of generative AI from Open AI LP, which can process and accept graphics as well as text inputs. What nobody, irrespective of their professional inclinations, can do anymore is avoid the ubiquitous and fast-growing presence of AI in business. It has already left an indelible mark on how we all operate, according to industry observers. As a result, generative AI may find a home in the arsenal of most engineers irrespective of age and longevity in the industry, they noted. It all comes down to the level of trust people have in technological innovations, according to the results of a survey conducted by Morning Consult.

"The base group, high in trust, has an almost blind faith in the technology, considering many haven't used a generative AI tool before," said Morning Consult analyst Jordan Marlatt, in a report. "The reach group — those who say generative AI outputs aren't remotely trustworthy — is the least likely to have tried generative AI. They tend to be slightly older than the average adult, but not by much. A third group, the swing cohort, constitutes everyone else. These are the people who are on the fence … This group accounts for a whopping 80% of the population, which isn't surprising: Generative AI is in such a nascent state that many people have yet to form an opinion on the technology, even if half of adults already believe it is here to stay."

The electronics design world is not taking a bet on generative

AI's future or viability. Like most people polled by Morning Consult, engineers are expected to be early adopters, partly because they cannot escape the growing tentacles of its reach and applications. This does not mean they are not skeptical of generative AI's broad application; they may just be more open to assessing it and learning from experience, Marlatt noted.

"There may be no group more excited by the prospect of generative AI than those working in tech, particularly in roles like software development and IT," he added. "Among software developers, 71% say workers in their field have more to gain than to lose from adopting generative AI tools, and 77% of IT specialists say that generative AI will create new types of jobs. About three-quarters of tech workers (74%) also say that embracing generative AI tools will be important to the future of their career."

Concerns about the use, reliability, and long-term utility of AI in the workplace have grown with the rapid adoption by many segments of the economy. For electronics design engineers, AI poses a significant dilemma; they are both its protagonists and its antagonists. They fostered its creation and must now try to manage – or even curb – its applications, power, and influence on growing areas of the economy. They are even being asked to help understand and improve the reliability of generative AI, and the extent to which users should depend on its output. The question is not whether electronics design engineers will use generative AI. The knotty issues revolve around how engineers will use it, for which applications and processes, and to what extent. Technology enterprises must also deploy generative AI in the design environment while preserving the unique mindset and independence of thoughts that engineers are reputed for.

Already in use

Many engineers in the semiconductor industry may have been quietly using generative AI for a host of other activities before chart GPT forcefully thrust itself into global consciousness. Companies like Nvidia Corp. said it has been working on generative AI for more than one decade and has now become one of the major providers of hardware and software products fundamental to the proper working of the technology. Generative AI will change the face of the design world and reshape how engineers relate to the existing resource ecosystem, the company noted. It will redefine how they source information, the speed with which they access data and other resources, and even alter the engagements with internal and external sources.

How will design engineers use generative AI? We identified seven possibilities:

1. Simulation and simulation evaluation
2. Research
3. Development of design solutions following engineering input
4. Further customization
5. Improving and accelerating tedious design processes
6. Creating and unlocking new products
7. Management of product obsolescence

Generative AI will not exist today without the innovations and huge processing powers unleashed by the electronics industry, especially semiconductor suppliers like Nvidia that supplies the advanced processors used by the data centers that support the sector. Nvidia executives said they foresee a new world of "accelerated computing and AI" emerging, enveloping engineers, developers, investors, and ordinary investors in a system marked by intense creativity and fast productivity fostered by a combo of semiconductors, other electronic hardware, and software.

As described by CEO Jensen Huang, a new future is unfolding, fueled by generative AI, and desired by all segments of the economy. Nvidia expects to be at the center of this new universe where all segments of the economy would be infused with and elevate artificial intelligence to a prominent role in all enterprise activities. Huang said AI will result in what he termed a "cloud first world."

Speaking at the company's recent GTS conference, Huang said: "We are at the iPhone moment of AI. Startups are racing to build disruptive business models, while incumbents are looking to respond. Generative AI has triggered a sense of urgency in enterprises worldwide."

What can engineers do with generative AI that they may not be doing now? It turns out that AI is non-discriminating. Engineers will have to accept that many of the functions they can ask AI to perform are like the ones non-technical users may also request. Some of the tasks AI will perform for users will encroach on what engineers currently do, according to Nvidia's Huang.

"Everyone can direct a computer to solve problems," Huang said, in his keynote speech at GTS. "This was a domain only for computer programmers. Now, everyone is a programmer. Generative AI is a new computing platform like PC, internet, mobile and cloud. And like in previous computing eras, first movers are creating new applications and founding new companies to capitalize on generative AI's ability to automate and co-create."

As if these challenges are not difficult enough, the high-tech community has also been dragged into the task of helping to answer ethical questions about how generative AI is used and who owns the intellectual property rights over the content or graphics created. They will have to attempt all these even as they try to resolve the same riddles in their own use of generative AI in both professional and personal settings.

The conclusion? Even if generative AI's usage results in engineers having to yield parts of their current turfs for those with interesting ideas but no engineering education, it will still help in advancing product development and expand the universe they and their employers serve.

How optoelectronics is enabling personalized smart homes

Roland Chapa, Technical Marketing Manager, Optoelectronics, TTI

Consumers have come to expect personalized experiences with everything they touch

Smart LEDs and sensor technologies are leading the way in customizing personal experiences in our homes, much like they're doing for productivity in many industries, which is leading to improved health, expanded living efficiencies, energy savings, and greater security.

As consumers, we have come to expect a personalized experience in nearly everything we touch: bots that react to information we provide them, unique profile settings in our vehicles and computers, and product recommendations based on our shopping histories. Data is the currency of the IoT and—as technology collects more bytes of information that learn our tastes—the quality and accuracy of suggested information improves.

The most logical extension of a personalized experience is the home. Where we live already reflects our décor style and tone; when guests arrive, they can instantly sense the environment in which the host prefers to live. Technology makes these choices a two-way street, like other technology-driven personalization experiences.

While many technological solutions deliver this customization, LED lighting and optoelectronics, in particular, can enable a high degree of personalization in the a smart home.

Smart home standards and challenges

Product designers focused on personalization should consider reviewing standards and innovations for smart homes.

The newest smart home standard, Matter **(https://bit.ly/41hpEDq)**, is a universal language integrating smart home devices. Developed by the Connectivity Standards Alliance, Matter will work on a local network, bringing the benefits of edge computing to smart home devices. It connects Thread (low power/bandwidth) for the optoelectronics with higher-power Wi-Fi and Ethernet for data-intense applications.

Most smart home devices operate in the 2.4GHz industrial, scientific, medical (ISM) band. With more connected devices, interference can be a problem. Insteon and Z-Wave operate below that range, at 915MHz, so having a mix of lower and higher frequency devices minimizes interference. Higher signal strength and low power operation can help reduce interference, as can testing and checking device locations in the home to optimize performance. An ISP-provided smart home hub—or web-based services like IFTTT or Stringify—are the best ways to network smart home devices to minimize interference.

Personalization through LED lighting

LEDs provide significant advantages over traditional incandescent and fluorescent bulbs. Beyond the energy efficiency, they last longer, provide improved lighting quality, and are inherently more customizable than their legacy counterparts. The color of an incandescent bulb depends on a precise filament temperature, while LEDs' color temperature is tunable depending on the phosphor formulations.

The next phase of innovation combines smart technology with LED lighting, creating "smart bulbs." These lighting solutions tie lighting to a control strategy like voice assistants or apps to enable user-defined environments. In addition, smart bulb LEDs easily integrate with existing fixtures, creating a connected device at each lighting location in the home. This benefit creates a personalizable network for users to operate from a single control point. Three applications of personalized intelligent lighting are setting control, zone control, and color and intensity.

Setting and zone control

The homeowner can save lighting settings for various events, such as "daytime," "movie night," or "entertaining." They can store a lighting color and brightness setting for one or more rooms under a single description and can activate the television or smart speaker at the same time. Setting control

allows the user to manually set the lighting to meet their changing needs.

Similar to controlling a specific setting choice, smart bulb controllers can operate independently of each other, creating various lighting zones throughout the home. An example of this function may be dimming lights in children's rooms while maintaining brighter lights in the kitchen in the evening. Additionally, home security, exterior, and patio lighting areas are customizable.

Color and intensity

Because a single filament color temperature does not govern LED color and intensity, a smart bulb offers various personalizable lighting options. For example, the lighting can be synchronized to the Circadian cycle, dynamically matching the color and intensity of interior light to the natural human frequency. In addition to improving sleep quality at night, this human-centric approach customizes LED lighting to enhance mood, concentration, energy, and alertness during the day by integrating technology with natural human tendencies.

Optoelectronics enhances personalization

LEDs are one type of optoelectronic device that deliver substantial personalized features. However, other related technologies magnify the effect by enhancing how LEDs can help. Among these are proximity sensors, optical displays, and communication tools.

Sensors

Innovative technology is only as good as the data it analyzes. As a result, sensors play a critical role in personalizing the smart home. For example, while the user can dictate the lighting color/intensity, optoelectronic ambient light and proximity sensors can detect these features, along with motion. Likewise, sensing a light condition can enable the home to automate light adjustment given a varying amount of natural light. Sensor-connecting lighting can also monitor the condition of a room and suggest or adjust settings according to a prescribed environment.

Optical displays

While apps or voice assistants provide familiar controls for monitoring and customizing the home environment, optical displays like organic LED (OLED) or LCD screens can provide a less disruptive method of communicating the devices' status to the homeowner. For example, a visual display can show real-time information to the homeowner based on data it collects, such as internal and external temperatures, and weather or home appliance metrics. It can also enable the user to manually change or override existing settings based on the display's information.

Communications features

Smart homes feel more personal when controls between connected devices are seamless. Optoelectronics delivers smooth communication between technology through infrared (IR) remote controls or visible light communication (VLC) from one device to another. Optimally, the user would act once—or not at all if sensors trigger a change—and the technology would instantly respond to a desired condition.

Energy efficiency and security benefits

While not necessarily active personalized functions, smart LEDs and optoelectronics can also add energy efficiency and security benefits for the homeowner. LEDs and optoelectronic sensors can detect opportunities to reduce the lighting amount, and they can connect to thermostats to govern energy usage and consumption. In addition, thermostats can "learn" user preferences, customizing the temperature setting for their typical schedule and optimizing energy efficiency in the process.

Personalized security is another application of optoelectronics to enhance the smart home. For example, instead of prompting the user to input a complicated code or risk an error de-activating an alarm, a system can employ facial recognition or biometrics to enable a minimally-disruptive security experience without compromising the benefits.

Takeaways

Today's consumers expect personalized experiences in their everyday lives. The home is no exception. Smart LEDs and sensor technologies are central to providing a customized experience that delivers additional benefits to enhanced customization, like improved health, energy savings and security. As a result, the utility of customized and smart lighting is transforming the industrial, retail, residential, automotive, and healthcare verticals.

Moreover, with the continued permeation of artificial intelligence, homeowners and professionals alike can enjoy a less active approach to controlling the home and office as the technology captures data and reacts automatically and dynamically.

www.tti.com

"With the continued permeation of artificial intelligence, homeowners can enjoy a less active approach to controlling the home as the technology reacts automatically and dynamically"

Porting ML models to custom AI HW accelerators

DeGirum's PySDK can help developers who wish to port ML models to custom HW

Upcoming hardware (HW) accelerators for edge artificial intelligence (AI) applications promise unprecedented efficiency in power, price, and performance. HW vendors generally couple their HW with software (SW) tools, illustrating applications that run out-of-the-box along with a collection of ready to use machine learning (ML) models.

While such models are sufficient to get started with the development process, application developers eventually want to port their own ML models that are customized and fine-tuned for their use cases. Porting ML models to custom HW poses a lot of challenges to the developers, primarily because the ML engineers involved in the model training might not be aware of the limitations of all the HW options available out there. The fact that not all HW can run all models is exacerbated by the rapid progress in model development where a new state-of-the-art (SOTA) is established every week.

The ML application pipeline

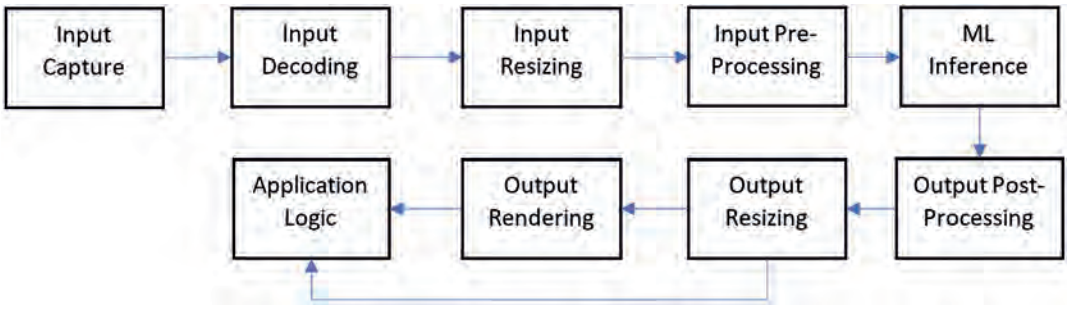
AI HW vendors typically provide model porting tools that convert trained ML models provided in the form of protobuffers or flatbuffers (ONNX, TFLite, etc.) to binaries that can be executed on the HW. They also provide a runtime that executes these model binaries. However, tools to compile a model and run the model binary alone are not sufficient for integrating the ML models to application SW. This is because the pipeline for an AI application is so much more than just ML model inference.

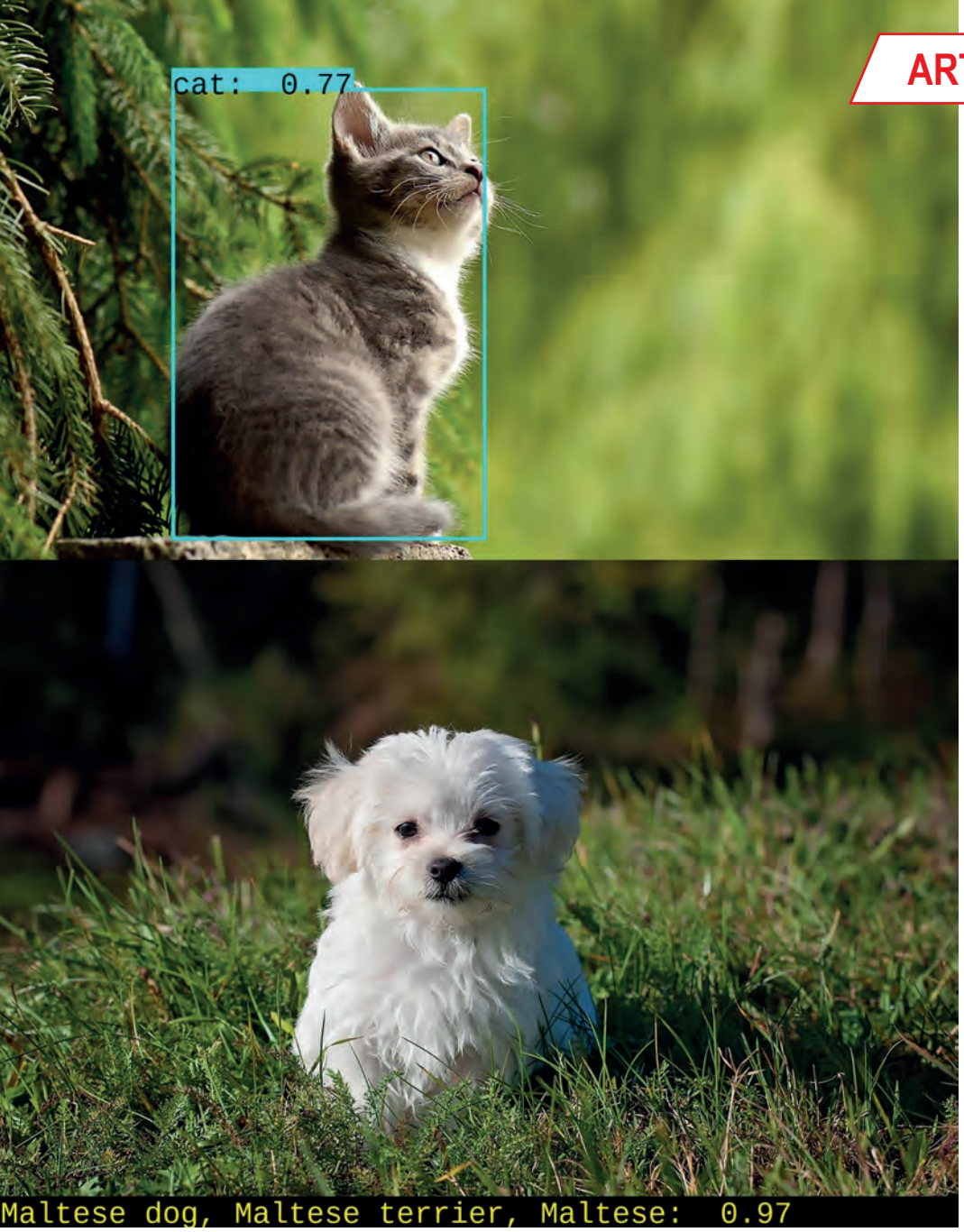
The first step in an AI application is capturing the input (image, voice, text) from the source. In the case of computer vision (CV) applications, the typical sources of input are cameras. Since cameras are used in a wide variety of applications, such as surveillance, quality control, and machine vision to name but a few, the format of the input varies depending on the type of the camera and the application. The incoming input stream can be encoded in H.264 or H.265 or MJPEG formats. Additionally, the resolution of the input can take one of the many possible values, such as VGA (640x480), 720p (1280x720), 1080p (1920x1080) and so on. Hence, the input needs to be decoded before it can be further processed by the ML models.

ML models are trained at some resolution (generally with square sizes such as 224x224, 416x416, and 640x640) which may not match the input resolution of the camera used in the application. The data used for model training comes from different sources and contains images of different sizes. Using square images while training allows the trained models to address different scenarios, as models can be trained at one resolution and deployed at a different

Shashi Kiran Chilappagari, Co-Founder and Chief Architect DeGirum Corp

A typical ML pipeline for a CV application





Visualizing outputs for (a) An object detection model, and (b) an image classification model

resolution. However, this means that the decoded input needs to be resized to the resolution at which the ML model is deployed. The inputs are often normalized before running the inference.

Different ML models provide different information about the input image. Classification models provide a list of most likely labels, whereas detection models provide labels for the objects as well as their location in the image. The location information is provided in the form of bounding boxes. This information is not the direct output of the model; it is obtained by processing the output of the model using methods specific to the model type. Classification models involve sorting the probabilities of the labels to find the most likely labels, whereas detection models need to decode bounding boxes and run a non-max suppression (NMS) algorithm to weed out extra overlapping predictions. The final predictions need to be resized to the original input size and then rendered for visual inspection or sent upstream so that application-specific logic can be applied to the output and proper action can be taken.

Challenges in model porting

Such a deep pipeline poses several challenges to the application developers, some of which are as follows.

#1 Replicating Model Accuracy: Developers want to ensure that the accuracy of the originally trained ML model is retained after porting it to custom HW. The model may undergo several optimizations before being compiled for the HW, and the developers need to be confident that such optimizations do not lead to loss of accuracy. However, replicating model accuracy after porting is a challenging task as the accuracy depends on a lot of implementation details listed below:

- Image Backend: The image processing library used to process the inputs. Examples include popular packages such as OpenCV and PIL.
- Interpolation Options: Options used for interpolating images when resizing the images to the size expected by the ML model. Most common options used include (a) nearest neighbor, (b) bilinear, (c) area, (d) bicubic, and (e) lanczos.
- Resize Options: Parameter that specifies how the image is resized to the size expected by the ML model and how the aspect ratio is handled. Common options include (a) stretching, (b) letterboxing, (c) cropping and then resizing, and (d) resizing and then cropping.
- Normalization: In some ML models, the input is normalized using per channel mean and standard deviation parameters before being sent to the ML inference
- Quantization: Model quantization can lead to smaller model size and faster inference (especially on custom HW). However, quantization can impact the model performance.

Developers need a SW stack that can take all these parameters into

Continues on page 28>

account to evaluate the performance of the ported model.

#2 Visualizing model output: To verify that an ML model has been ported successfully, developers need SW to visualize the output of the ML model on some sample inputs. Since different types of models provide different information, a lot of boilerplate code is needed to visualize the model output. Image classification models provide top labels for the image, object detection models provide bounding box information for various detected objects in the image, pose detection models provide key-point information, and sematic segmentation models provide per-pixel class label information. Rendering these different types of information requires developing code specific to handling these cases.

#3 Handling multiple HW options: Consider a scenario where an application developer wants to evaluate multiple HW options and choose the HW best suited for their use case. In such a scenario, they have to develop multiple SW stacks, each one addressing a different HW option. This is due to the fact that the model porting tools—along with the inference runtime libraries—are HW specific. Once they've developed the application, they need to evaluate all the options and then pick the right HW. This leads to a lot of wasted time, effort, and money as bringing up custom HW is a long, expensive, and frustrating experience.

#4 Optimizing Performance: Employing a multistage pipeline in the application has implications on the overall performance as each stage needs to be pipelined efficiently. Different stages may utilize different HW resources (such as video decoders, ML accelerators. etc.), which further complicates the optimization process. In order to utilize the AI HW accelerator resources efficiently, developers need to carefully analyze the various stages and orchestrate the application's execution so that the final application is stable and efficient. Executing each stage of the pipeline in a single synchronous thread will lead to high latency and poor utilization of HW resources.

DeGirum's PySDK

DeGirum's python software development kit (PySDK) is specifically designed to address the challenges faced by application developers. Instead of just providing an inference runtime library that focuses on running the ML model inference, the PySDK provides a simple Model Predict API that handles the pre-processing of the input (including resizing and normalization), the ML inference, and the post-processing of the output (including rendering predictions on original image).

The PySDK also provides a highly efficient Batch Predict API that pipelines all stages of the application, including input capture and decoding as well as running the application logic. The PySDK manages all the ML inference calls to the AI HW and ensures that these calls are scheduled in such a way as to maximize the HW usage. Other highlights of the PySDK include:

- A single JSON file that specifies all the parameters related to input pre-processing, ML inference, and output post-processing. This greatly helps the model developers to replicate model accuracy benchmarks on the ported model.
- A Model Predict API that handles overlaying predictions for different model types such as image classification, object detection, key-point detection, and sematic segmentation. This feature obviates the need to develop boilerplate code for various common use case.
- HW agnostic APIs that ensure that the same code works for multiple HW options. This allows developers to create a unified SW stack that can be used to evaluate multiple HW options and pick the best suited option.

The simplicity of the Model Predict API can be illustrated using the code snippet below:

```
import degirum as dg
zoo=dg.connect_model_zoo()
model=zoo.load_model('yolov5_n2x_orca')
res=model(image)
res.image_overlay
```

This code illustrates a YOLOv5 model running on DeGirum's ORCA HW. By changing the model name, the same code can be used to run other types of models. Also, the same code can be used to run across different HW options.

Porting ML models to custom HW poses a lot of challenges to the developers, but DeGirum's PySDK can help smooth the way.

www.degirum.com

"DeGirum's python software development kit (PySDK) is specifically designed to address the challenges faced by application developers"

Operational amplifiers for piezoelectric actuators

It's important to follow sound principles with respect to any driving circuits used with these devices

Over the past few decades, the use of piezoelectric actuators has seen a growing increase in popularity. This is due to the many advantages these devices offer, some of which are as follows:

- No moving parts: This makes motion in the sub-nanometer realm possible.
- Fast response: Microsecond response times with acceleration rates of more than 10,000g.
- High force generation: Capable of moving loads of several tons.
- No magnetic fields: Piezoelectric actuators produce no magnetic fields, nor are they affected by them.
- Low power consumption: Static operation consumes virtually no power.
- No wear: No moving parts such as gears or bearings.
- Vacuum and clean room compatible: Piezoelectric actuators cause no wear and do not require lubricants.
- Operate at cryogenic temperatures: The piezoelectric effect continues to operate at temperatures approaching zero degrees kelvin.

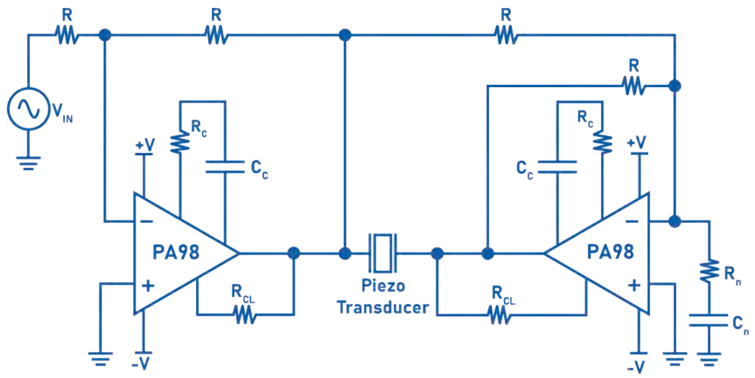
Using piezoelectric actuators can provide many benefits, but it is crucial to keep some essentials in mind when designing systems that employ these components.

Limited strength in tension: The tensile strength of a cylindrical piezoelectric actuator is approximately 10% of its strength in compression. It is essential to abide by these values to avoid fracturing the piezoelectric actuator. Specific values can be obtained from data sheets supplied by the piezoelectric actuator manufacturers.

Boundaries on acceleration: When driven by a periodic waveform, the acceleration will increase exponentially with frequency. So, it is important to identify the upper limit of the device's ability to withstand high acceleration forces. In particular, multilayer piezoelectric actuators are vulnerable to delamination should their acceleration limits be exceeded.

Driver circuits do consume power: As was noted earlier, piezoelectric actuators consume virtually no power when static, other than the quiescent power consumed by the electronics. However, the power dissipation demands from any power operational amplifier circuits when the actuator is driven can be significant indeed.

Follow sound principles
It's important to follow sound principles (no pun intended) with respect to any driving



circuits. Make sure the driving power operational amplifiers are working in their safe operating region and current limiting is provided to protect the circuitry from an inadvertent short circuit. Other essential design tasks include selecting a satisfactory heatsink, flyback diodes, and compensation capacitors.

Piezoelectric applications are commonly driven with higher voltages (typically greater than 50V). For this purpose, Apex Microtechnology offers high-performance power operational amplifiers ranging from 50V to 2500V. One such example is the PA98. This 450V, 200mA high-power operational amplifier with an impressive 1,000V/µs slew rate is targeted for high voltage applications including piezoelectric transducers, electrostatic transducers, and deflection.

The PA98 series is a hybrid product design housed in a space saving, electrically isolated 12-pin PowerSIP package, which lends itself to high-density circuit board layouts. Please visit our website to view our full product portfolio, including the PA98.

www.apexanalog.com

"Using piezoelectric actuators can provide many benefits, but it is crucial to keep some essentials in mind when designing systems that employ these components"

Micron to build memory megafab in New York

Leading-edge megafab will create nearly 50,000 New York jobs

Micron Technology, one of the world's largest semiconductor companies and the only US-based manufacturer of memory, plans to invest up to $100 billion over the next 20-plus years to build a leading-edge memory megafab in New York. This megafab, which will create nearly 50,000 New York jobs, is the result of the bipartisan work of Congress and the Biden Administration to pass the CHIPS and Science Act.

Building the workforce of the future

Both traditional and non-traditional workforce development pathways are critical to train the workforce at the scale necessary for the US semiconductor industry. The workforce of the future will require talented engineers and technicians with diverse skill sets to manage and operate state-of-the-art cleanroom facilities and develop advanced engineering solutions. Micron is committed to make these careers accessible to all, particularly to individuals in underrepresented and rural communities.

Investing in STEM education

STEM education in K-12 through post-secondary schooling and training programs is essential to create a skilled talent pipeline. Micron will invest in local education programs and empower under-resourced youth to pursue careers in STEM to support building a more diverse and inclusive technology industry at large.

As part of Micron's commitment, the company will invest $10 million over 10 years in the Syracuse STEAM school—the first collaborative school in the area designed to integrate the areas of science, technology, engineering, the arts, and mathematics—as well as other K-12 programs in the region to reach historically marginalized students and reduce barriers to future STEM careers.

Engaging with local communities

Micron prioritizes investing in and enriching the communities where its team members live and work. In support of childcare and early childhood readiness programs, Micron will make an initial $500,000 investment in the YMCA of Central New York. This investment aims to expand access to high-quality childcare and early learning for underserved communities in the region. Micron will continue to partner with the YMCA and other organizations to identify future investments that empower children and families and build an equitable and inclusive community for all.

Additional Micron commitments

Micron will continue evaluating ways to support the Central New York region to cultivate the next generation of talent, accelerate economic opportunities for underserved communities, support the region's infrastructure, and build a diverse labor pool.

In line with this extended commitment, Micron will establish Syracuse University's Future-Ready Workforce Innovation Consortium at the College of Professional Studies. In partnership with the Central New York business community, trade unions, community colleges, and other four-year institutions in New York State and beyond, Micron will collaborate with Syracuse University to implement a multidimensional and inclusive approach to workforce development, upskilling, and professional retention.

www.micron.com

IPC issues report: March Global Sentiment of the Electronics Supply Chain

Despite growing economic uncertainties, the electronics manufacturing industry remains upbeat

Per the IPC's March 2023 Global Sentiment of the Electronics Supply Chain Report **(https://bit.ly/42Wr9IU)**, the past month delivered another month of stable industry sentiment: industry demand appears to remain intact, production holds steady, and some labor challenges may be receding.

Although overall sentiment is upbeat, roughly 58 percent of sentiment survey respondents expect to raise prices in 2023 with an average of an 8 percent increase. Among other data, survey results show the following:

- Labor costs, orders, customer inventory, backlogs, and ease of recruitment is expected to remain relatively stable.
- Backlogs are rising more so in North America when compared to both Europe and APAC. Nearly two-fifths (38 percent) of firms in North America indicate backlogs are on the rise, while a significantly lower 8 percent of European firms and 14 percent of those in APAC are experiencing a current increase.
- Material costs are declining at a faster pace among manufacturers in Europe vs. those in North America. While 11 percent of firms in Europe indicate material costs are currently declining, 0 percent of firms in North America are presently reporting a decrease.
- The majority of manufacturers indicate less than 10 percent of 2022 revenue growth was attributable to pricing impacts, which holds true for manufactures in North America, Europe, and APAC.

For the report, IPC surveyed hundreds of companies from around the world, including a wide range of company sizes representing the full electronics manufacturing value chain.

About IPC

IPC is a global industry association based in Bannockburn, Ill., dedicated to the competitive excellence and financial success of its more than 3,200 member companies, which represent all facets of the electronics industry, including design, printed board manufacturing, electronics assembly, and testing. As a member-driven organization and leading source for industry standards, training, market research, and public policy advocacy, IPC supports programs to meet the needs of an estimated $2 trillion global electronics industry.

www.ipc.org

Adapting to faster paced development cycles

Increasing complexity in embedded devices requires a smarter approach during software development

The level of complexity of embedded devices continues to increase unabated. At the same time, the pressure to reduce development times is high. This situation is alleviated by implementing strategies for increased code reuse and more efficient development/debug tools for embedded developers. This Part 1 of a two-part discussion looks at the use of an adaptation layer approach to increase code reuse.

An adaptation layer is a software layer that provides a standard software interface between various layers of software and the hardware interfaces of an embedded device. This enables many software components to be reusable, e.g., the same application or wireless software stack to run across a wide range of platforms with different CPUs and real-time operating systems (RTOSes), thereby enabling software reuse and providing significant time savings when compared to traditional porting environments.

Clarinox Technologies is company that specializes in developing software solutions for wireless communications. Clarinox has implemented an adaptation layer, SoftFrame, to facilitate a standard interface for the Clarinox wireless protocol stacks (Bluetooth and/or Wi-Fi). This upper layer wireless protocol stack is a set of software layers that provide the functionality required for Bluetooth or Wi-Fi wireless communication. It is responsible for managing the transmission and reception of data between wireless-enabled devices based upon relevant standards (Bluetooth SIG, IEEE802.11 and Wi-Fi Alliance).

SoftFrame is designed to be flexible and customizable, allowing it to be adapted to a wide range of hardware devices and operating systems. It supports various Bluetooth Classic and LE profiles, including LE Audio as well as the Wi-Fi protocol.

One of the main benefits of SoftFrame is that it simplifies the integration of Bluetooth and/or Wi-Fi functionality into devices. It reduces the development time and cost by providing a standard interface that can be integrated into the operating system or middleware of a device. This means that device manufacturers can focus on developing their core functionality without having to worry about the complexities of the Bluetooth and Wi-Fi standards or any changes required for the next generation of the same product.

In addition, SoftFrame provides the ability to reuse the stack and application software resulting in time tested software running in millions of devices in the field providing confidence in the robustness and reliability of the software, which is critical to many embedded applications.

SoftFrame is also designed to be scalable, allowing it to be adapted to devices with different processing power and memory requirements from M0 up to high-end multicore devices; and from small RTOSes to complex operating systems. SoftFrame's modularity enables it to cater for different configurations to tailor to the specific needs of a device supporting multiple TCP/IP and RTOS/OS.

Another advantage of an adaptation layer is to include a debugging and testing architecture customized for wireless embedded systems. Wireless devices have specific needs as they are harder to debug and test due to the dynamic nature of the communications and the complexity of the Bluetooth and Wi-Fi standards.

Overall, Clarinox believes that an adaptation layer is an essential software component for enabling the efficient addition of wireless functionality in devices. It simplifies the integration of Bluetooth and Wi-Fi technologies, provides interoperability between devices, and ensures high performance, and scalability. As the use of Bluetooth and Wi-Fi technologies continues to grow, SoftFrame will play an increasingly important role in enabling seamless communication between devices.

Trish Messiter, CEO
Clarinox Technologies

www.clarinox.com

"The SoftFrame adaptation layer is designed to be flexible and customizable, allowing it to be adapted to a wide range of hardware devices and operating systems"

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Software-defined vehicles are here

The advent of software-defined vehicles signals big changes for semiconductor manufacturers

The automobile industry is seeing a seismic shift, transforming from internal combustion vehicles to ones with electrified drive trains that are software-centric. This transition is doing more than changing how cars move—it is also changing how they operate.

These new vehicles, which are known as software-defined vehicles (SDVs), are increasingly more akin to cell phones on wheels than the gas-powered cars of yesteryear. Like cell phones, for example, SDVs fully integrate into their driver's digital existence.

These vehicles introduce connectivity, automation, and personalization features through over-the-air (OTA) updates, which are new to the automotive space but familiar to mobile computing and telephony. Where car personalization was, until recently, defined by hardware, it will now be defined by software that can be updated, upgraded, and—one day—sold separately from the vehicle itself.

These vehicles will change everything in the transportation sector, including how cars are made, how they're sold, and how they're operated. SDVs will introduce significant challenges—and major opportunities—for suppliers as well. Specifically, semiconductor manufacturers, as these cars are more data and processing intensive than any of their predecessors.

What's driving the adoption of SDVs?

There are several trends driving demand for software-defined vehicles as follows:

- **Autonomous Operation:** The era of self-driving cars is not yet here. To be sure, there are numerous autonomous functions that the current crop of SDVs offer drivers, which improve the driving experience and safety considerably. These autonomous functions focus on advanced driver assistance systems (ADAS), such as adaptive cruise control or lane assistance on the highway. Multiple sensors power these functions, including cameras, mmWave radar, lidar, gyroscopes, and GPS.
- **Easier Maintenance:** A car's operating system can leverage sensor, historical, and driver data to forecast part failures accurately. This increased certainty and safety, combined with the power of OTA preventive maintenance and remote diagnostics, can significantly lower the total cost of ownership (TCO) for car buyers.
- **Higher Gas Prices:** Hybrid vehicles offer improved gas mileage, while EVs eliminate the need for gasoline. These benefits aside, SDVs promise digitally interconnected systems to optimize efficiency.
- **Increased Personalization:** A new generation of car buyers prioritizes functional personalization and connectivity of their vehicles instead of focusing on traditional measures like horsepower or external styling. This demand for software-led personalization has made the in-car experience a key battleground for automotive manufacturers to differentiate themselves.

The collection and interpretation of data—collected from both sensors and the driver—support all these benefits.

Jim Schwartz, Senior Director, Automotive Software & Electronics, NI

Silicon behind the wheel and under the hood

An SDV requires multiple controllers to oversee different vehicle functions. For example, one controller might control the car's interior lights and door locks, while another might focus on managing power consumption.

Beneath these controllers, there may be hundreds of microcontrollers integrated into electronic control units (ECUs) throughout the vehicle, each supporting single-function operations. For instance, there might be a microcontroller inside each headlight, one controlling each door lock, and so on.

The numerous sensors and actuators required throughout an SDV need a powerful computing architecture featuring both centralized and distributed processors.

This amounts to many chips—ones that require a great deal of functionality and reliability—since failures could be catastrophic.

In addition to reliability, there's an increased emphasis on creating multi-use chips that can be applied to multiple uses and environments to maximize economic opportunities for chip manufacturers. Today, this means you might find the same modem in a 5G phone and the dashboard of a car. By extension, this means that, for many semiconductor manufacturers, every chip needs to have the same reliability baked in, since that chip could end up in a vehicle.

Testing is critical

Chip testing has become a critical component of the automotive industry's efforts to ensure the reliability and functionality of its products.

To survive and thrive in the fast-paced world of semiconductor manufacturing, companies need to adopt new strategies and approaches, including the following:

- **Test Automation:** Given the high volume and increased complexity of chips, there has been a move away from manual testing of repetitive measurements. By utilizing automated testing that taps software-defined functionality, chipmakers can cover more test cases than organizations doing testing manually, and they can do it faster.
- **Standardization:** Companies must be able to compare test results across the company, ensuring apples-to-apples comparisons. Standardizing on common test hardware and software platforms makes these comparisons easier and makes testing go faster. Organizations with standardized test systems report that new teams can go from receiving a part to producing a test report much more quickly.
- **Digital Transformation:** Centralizing data and analysis allows companies to compare measurement results through simulation, validation, and manufacturing steps. Centrally storing and managing data lets manufacturers find data when and where it's needed, providing context for analysis. Central management of test data is often a critical step that enables manufacturers to use test results to improve product designs, and it is often a key digital transformation initiative in both semiconductor and automotive manufacturing organizations.

While test automation has obvious benefits, including speeding up testing processes and adding scalability and efficiency, it is just the first step. Chip manufacturers must embrace standardization and centralization of their data—becoming true data- and analysis-led organizations—to handle the increased demands of providing chips to the transportation sector.

Big (but not easy) money

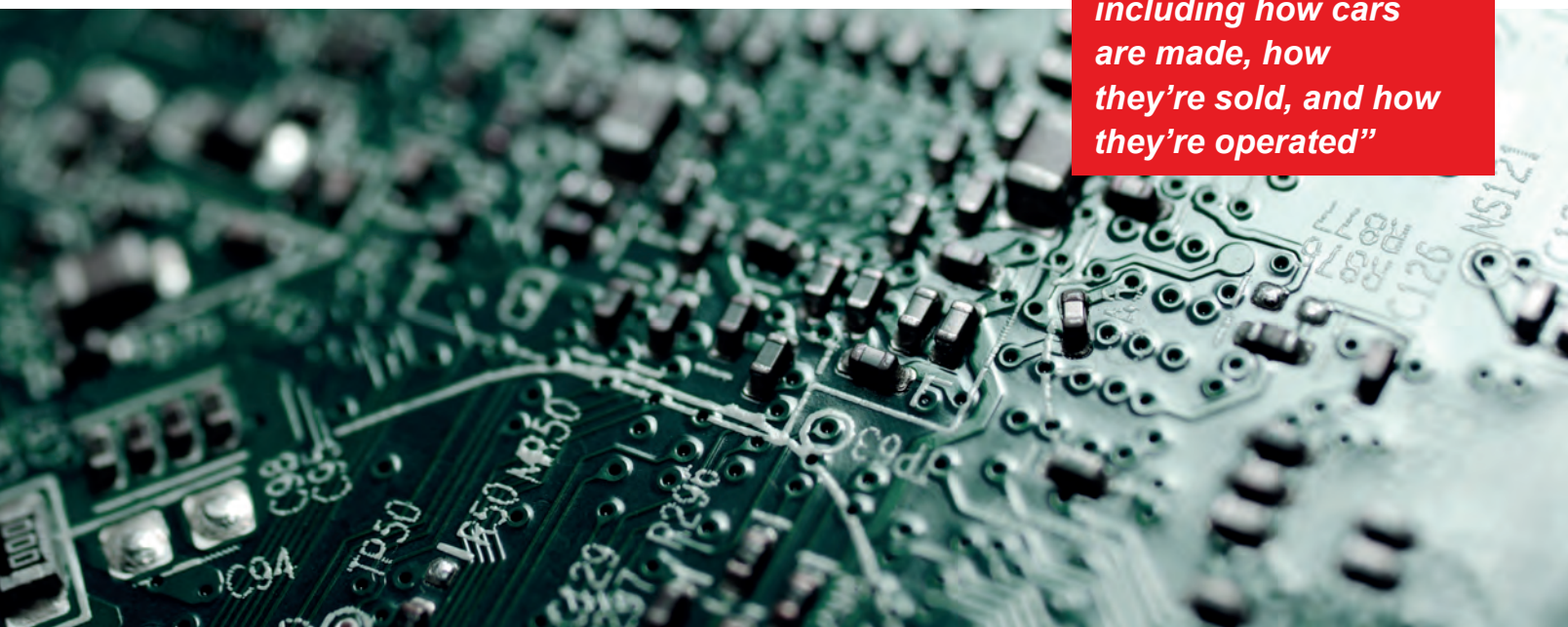
The impact of SDVs on the semiconductor industry is significant and multifaceted. In addition to testing and increased demand for chips with robust functionality, chip manufacturers will need to explore other structural changes to adapt to this challenging and rewarding environment.

In time, we will likely see escalating collaboration between chipmakers and automotive manufacturers. With software playing an increasingly important role in the automotive industry, semiconductor manufacturers and automotive manufacturers are likely to collaborate more closely to develop solutions that meet the needs of both sectors.

Given the fact that SDVs are a relatively recent phenomenon; there is still plenty of room for innovation, and the opportunity for winners in this space is immense. Analysts put the increase of the automotive semiconductor market in North America at a compound annual growth rate of 9.82% between 2022 and 2030 to reach a whopping $57 billion. As a result, semiconductor manufacturers are likely to invest more in research and development to meet the demands of this new market.

www.ni.com

"Software defined vehicles will change everything in the transportation sector, including how cars are made, how they're sold, and how they're operated"



Short circuiting the prototyping design cycle

Many companies and developers are moving to a "fail fast" philosophy

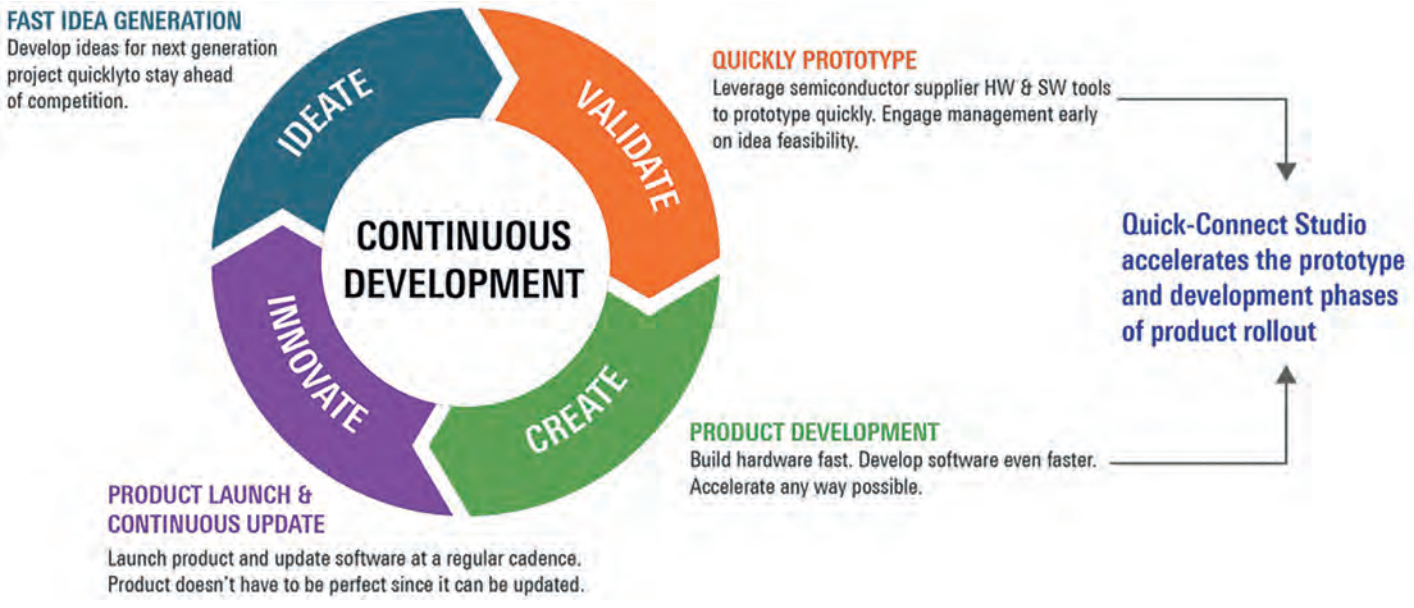
Getting an electronics product to market is significantly different than it was just 10 years ago. On top of the normal advancements in hardware electrical components, and the increasing density and performance improvements of microcontrollers and microprocessors, the exponential change in difficulty has been squarely focused on software.

The two biggest factors leading to this rapid change in software development have been the opening of the mobile phone app store and the ubiquity of wireless connectivity. These two technologies have simultaneously made our devices richer and more fulfilling, but also have increased the complexity of the products and the engineering work behind them. Let's look at how a compressed product design cycle and these changes in software development have increased the load on engineers and what tools exist to provide relief.

In the case of traditional serial development flows, once a new product plan has surfaced, a significant amount of time is spent refining the idea, developing hardware, working on software, and finally producing a product that is introduced to the market.

Today, many companies and developers are moving to a "fail fast" philosophy, where idea generation, testing, and market validation are compressed into a tight loop to achieve the desired outcome, which would be acceptance by the market of a particular product or service. In this case, skunkworks engineering teams continuously build out, test, and develop product proof of concepts (PoCs). Rapid prototyping with development kits, open-source solutions, and tried and true breadboarding allows software engineers to quickly test out new device firmware that can easily show how the end product will look and feel. If successful, they can move on to quickly develop a product and get it to market ahead of the competition. This process then repeats itself on the next product.

As mentioned above, the issue for software developers lies in the connection to the outside world. If we look back to even a short decade ago, many devices performed their tasks in unconnected isolation. There were fewer mobile apps to control and interact with them. Updates, if any, were mostly done via USB, and the PC-based applications used to perform these updates were sketchy



at best, with warning windows screaming at you to make sure your computer does not disconnect or lose power or else you will end up with a bricked device. Given this, the software for these products was more robust, knowing that there may not be a way to update it in the future.

Fast forward to today, and most devices on the market are connected via Bluetooth or Wi-Fi to either a mobile phone or local network. Low-cost and low-power LTE, Cat-M1, and NB-IoT are becoming more popular for always-on connections. Software knowledge of these new stacks and communication protocols means that engineering effort now shifts from bare metal code to utilizing an RTOS like FreeRTOS from Amazon or Azure RTOS from Microsoft. Engineers must ramp up their knowledge base and design mentality to develop in a threaded environment.

These constant connections to the outside world now bridge an embedded device with mobile applications, cloud services, AI/ML toolchains and algorithms, and wireless over-the-air updates. This has a few negative drawbacks. New tools need to be downloaded and installed, and sometimes finding these tools can be difficult, especially in new technology areas where there are typically many different offerings since the market isn't settled yet. On top of bulky tool installation, the biggest hurdle is learning different technologies. Many of these technologies look and feel completely different than working with standard C, and the context switching introduces inefficiencies. The time it takes just to show a working demo or PoC starts to compound as we add in additional pieces.

One thing should be clarified at this point. All engineers working on a product must have intimate familiarity with all the components in the design. Software engineers must understand how to communicate with the different buses inside the device, and they must know how to create threads and interact with them. But the barrier our industry needs to overcome is burdening engineering staff with becoming experts at the very beginning of the design cycle in order to use a demo project or see a device operating. Engineers must be comfortable that the selected devices can achieve their vision for their product, and seeing is believing. After you are comfortable that all the components can satisfy your needs, then the engineering staff can take the proper time to study and learn everything about the components to maximize and extract every bit of performance out of them.

In true engineering fashion, where a problem exists, solutions tend to bubble up to the top to solve them. Accelerated software development tools, such as Renesas' Quick-Connect Studio (QCStudio), aim to lower the development bar during the prototyping stage.

This online tool allows you to drag-and-drop components at the solution level. Once you are happy with the components that have been selected, Quick-Connect Studio can automatically configure the devices and generate the first working project utilizing those components. Software engineers do not have to learn about complex pin muxing, port connections, or register setups just to try out a prototype. The tool is a full-fledged IDE and code can be modified directly in the browser. Since Quick-Connect Studio is cloud-based, compilation is done remotely on a resource rich and powerful cloud server, thereby cutting down on the need to have a powerful desktop or laptop PC. Once compiled, the engineer sets up their hardware exactly as depicted in Quick-Connect Studio, downloads the binary image, and can immediately see the results.

"Accelerated software development tools aim to lower the development bar during the prototyping stage"

Embedded engineers face many challenges in getting a product to market. As software and systems become more complex, the need for efficient and tighter design cycles will only grow. By embracing agile methodologies, reusing common frameworks and architectures, and using automation tools, software and systems engineers can keep pace with the dynamic nature of the industry and deliver higher quality products in less time.

www.renesas.com

Improving accuracy when calibrating high voltage systems

Using advanced high voltage meters improves accuracy and offers a portable, simplified solution

When working with test and measurement equipment to calibrate high voltage systems, electrical and test engineers typically use external probes such as high voltage dividers. However, these instruments are prone to errors that can lead to imprecise readings. This article describes an alternative approach to measuring high voltage systems that employs advanced high voltage meters.

Measuring high voltage systems

High voltage applications span numerous industries, from high-tech, medical, and automotive, to industrial manufacturing, research labs, aerospace, and many more. The high voltage systems used in these applications include:

- Switchgear
- Switches
- Power transformers
- Instrument transformers
- Reactive power equipment
- Insulators
- Control equipment
- Relay panels

Measuring high voltage systems during design, manufacturing, and in calibration labs is essential for meeting various global reliability and safety standards, as well as manufacturers' warranty requirements. The high voltage test and measurement instruments used for this calibration include:

- Meters
- Voltage dividers
- Power supplies
- Signal sources
- RF power amplifiers
- Hipot testers
- Oscilloscopes

This article focuses on two such high voltage test and measurement instruments: meters and voltage dividers.

Voltage dividers

Voltage dividers are external probes commonly used to measure higher voltages. For example, a 100:1 voltage divider allows an instrument with a 1kV (max) input to measure an applied voltage of up to 100kV. Composed of many carefully matched resistors, a voltage divider will (theoretically) eliminate errors from self-heating or other factors that affect the resistor string in a uniform fashion. However, there remain a number of contributing factors to error and uncertainty when using a voltage divider, including:

- Resistance variation from one resistor to another
- Variations (although minor) in temperature coefficients
- Electromagnetic effects
- Capacitance effects
- Variations in meter input impedance, which necessitates it must be calibrated with the meter

Advanced high voltage meters

Today's advanced high voltage meters, such as the Vitrek 4700 Precision HV Meter, allow test engineers to directly measure voltages up to 10kV (10m kV DC or RMS AC) without using external probes. This meter offers performance that rivals traditional high voltage reference dividers but—unlike using a divider—it provides instant and direct high voltage measurements in a portable bench-top enclosure. This meter is capable of meeting the following high voltage specifications:

- Base accuracy: 0.03% DC, 0.1% true RMS plus limitations and adders (no range adder needed): Maximum voltage: 10kV DC, 10kV AC RMS
- Impedance: 110MΩ
- Ranging: None
- Noise Floor: 30mV
- Frequency response: 0.01Hz to 600Hz

  Offsets: Up to 800V
- Differential measurements if two external probes are used

To extend high voltage measurements beyond 10kV up to 150kV, SmartProbes can be added to the 4700. Unlike voltage dividers that must be calibrated with the meter, these probes store their own calibration data, which is downloaded when plugged into the meter.

Conclusion

The typical approach of employing a voltage divider network when calibrating high voltage systems comes with drawbacks, such as introducing error-producing effects like self-heating, capacitance effects on AC measurements, and electromagnetic effects. In contrast, using advanced high voltage meters improves accuracy and offers a portable, simplified solution.

www.vitrek.com

Verifying multi-threaded embedded systems with software tracing

Traditional verification methods are not sufficient to fully verify multi-threaded systems

Most embedded systems today are powered by multi-threaded software, e.g., running on Linux or a real-time operating system (RTOS). While multi-threading has many advantages over single-threaded designs, it can make the software more complex and the verification more challenging.

Traditional verification methods like code review, static analysis, and functional testing are necessary but not sufficient to fully verify multi-threaded systems where there is an intricate web of dependencies between threads caused by explicit and implicit thread interactions.

Moreover, such dependencies can be affected by software execution time variations, which are not explicit in the code but rather an emergent behavior in runtime. Timing effects on thread interactions are often an uncontrolled factor when testing multi-threaded systems, so even vast amounts of testing might skim only the surface of an ocean of potential execution scenarios. As a result, latent defects may remain undetected, only to surface following deployment. Embedded software often also needs to meet real-time requirements. For example, a control system might have a requirement to output control signals to a motor controller every 5 milliseconds, where any additional delay is considered a failure. Such requirements are not only affected by the execution time of the specific thread, but also by dependencies on other threads. Thus, verifying real-time requirements is about more than measuring timing metrics. It is also about identifying potential risks from thread interactions that may affect the timing requirements.

So, how do you verify that a design is good from a multi-threading perspective? The de facto solution is runtime observability using software tracing. Percepio Tracealyzer offers a large set of visual analysis features and functionalities for software design analysis and verification of real-time requirements. By adopting system tracing with Tracealyzer, developers can:

- Collect detailed runtime data on thread execution, thread interactions, and timing over long test runs, without needing any specialized hardware for this purpose.
- Find anomalies in the real-time behavior using various high-level overviews, such as the CPU Load Graph or the statistics report, and simply click on an abnormal data point and see the details in the execution trace view.
- Analyze software timing variations, for example using the Actor Instance Graph showing a plot of various timing metrics for each thread over time.
- See thread dependencies, for example using the Communication Flow Graph that provides a visual overview of thread interactions through IPC objects.

Tracealyzer does not require any particular hardware support, but instead relies on efficient software instrumentation in the target software. The trace data can be transferred to the host computer in various ways, for example by real-time streaming over an ethernet connection or a supported debug probe.

To learn more about Tracealyzer and to try the free evaluation, please visit the Percepio website.

www.percepio.com

Miniature AC/DC converters for smart home applications

The predicted growth in smart homes promises opportunities and challenges

As “always-on” appliances are proliferating in every aspect of people’s daily lives, homes are becoming smarter. According to Statista (www.statista.com), the total revenue generated by companies servicing the smart home market was approximately $100 billion by the end of 2022.Furthermore, the percentage of smart homes is expected to grow from 5.5% in 2022 to 14.8% in 2026.

This predicted growth promises opportunities to the creators of smart home products. However, as is usually the case, opportunities and challenges go hand in hand. While customers are always going to be attracted by low prices, they also demand good performance and high reliability. In addition to small space constraints, appliances of this type must often accommodate long standby times. Meeting all these needs—size, performance, and price—at the same time is a big headache for manufacturers!

MORNSUN is an innovative power supply manufacturer and designer that has been in the power supply field for 25 years. With more than 6,000 high-quality products on the market, MORNSUN still invests substantial R&D resources in developing new power supplies to address the challenging requirements of the latest technologies in different industries.

In the case of smart home applications, for example, MORNSUN offers a series of flexible LS-R3 open-frame AC/DC power supplies. The LS-R3 series offers a wide-power selection range of 1-15 watts. With a static power consumption of 0.1W, these modules work with a wide power range, with high and low loads at 85°C, up to 50% load.

With the LS-R3, users can select peripheral components based on their unique performance, cost, and space goals, as opposed to being subject to the circuits and components chosen by the power supply manufacturer. In the case of applications with limited space and less stringent EMI requirements, for example, filter components with large layouts and high prices can be replaced with common mode chokes and inductors. In this way, developers have greater control over the cost of their end system.

For developers having problems with their peripheral designs, MORNSUN also offers integrated power supply solutions to reduce the pressure of time and cost, such as the onboard DIP AC/DC converter LD-R2 series, for example.

The LD-R2’s input range is different from the traditional product’s 264V because it’s been upgraded to span 85-305V, which is more reliable in appliances. What’s more, in addition to a wide-power selection range of 3-90 watts, these modules, which are ideal for applications with space limitations, feature a 2-Y-capacitor design, satisfy EMI Class B without requiring external components, and provide no-load power consumption as low as 0.1W.

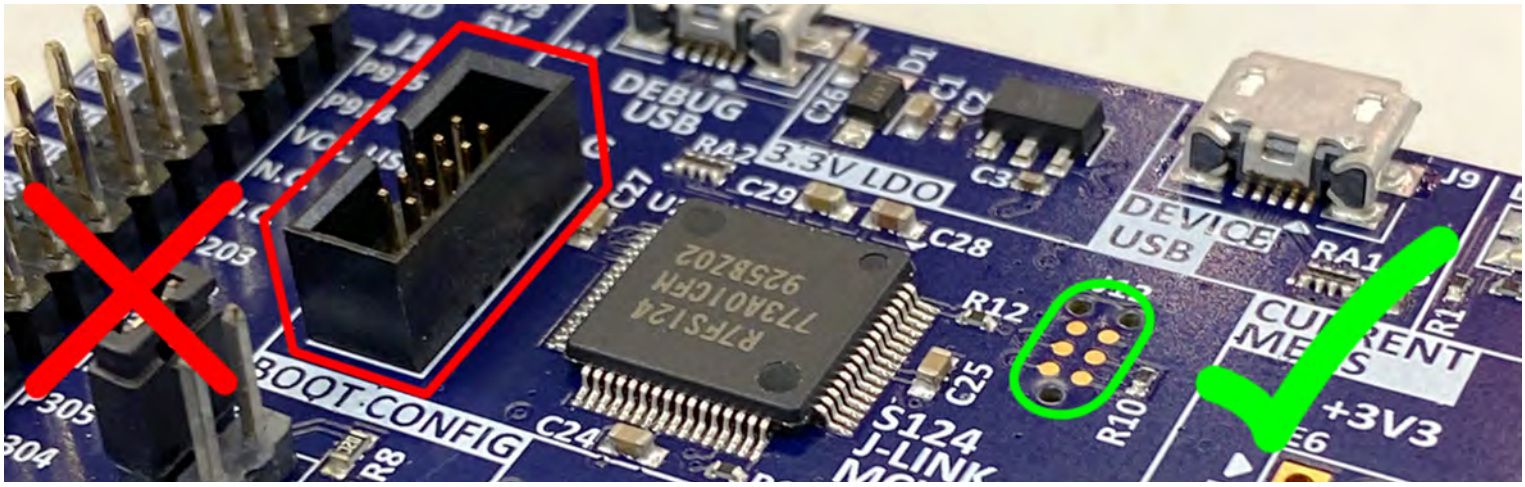
Developers based in North America can search for “MORNSUN” in the Digi-Key online catalog where they can obtain more information and complete their orders in seconds.

www.mornsun-power.com

The LS-R3 open-frame AC/DC power supply

The LD-R2 onboard DIP AC/DC converter

Tag-Connect



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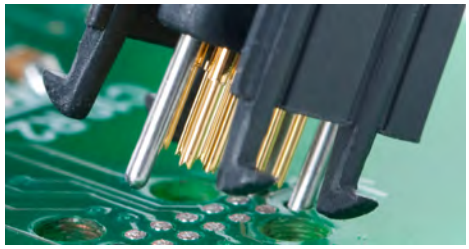
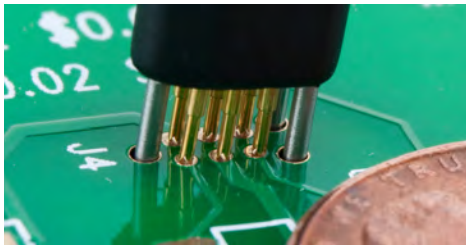
JTAG Connector Plugs Directly into PCB!!



Legged version snaps into the board



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STLink-V3 for illustration only

Non-contact body temperature measurement

Using an enhanced non-contact methodology to make skin thermometry more accurate

Joris Roels, Marketing Manager, Melexis Microelectronic Integrated Systems

In today's modern society, we are now much more aware of the need for a better understanding of our health and wellbeing. Body temperature is one of the essential parameters via which assessments can be made, and this article discusses the most effective ways of doing this to a high degree of accuracy. In particular, we look at the role consumer electronics is set to play.

The capturing of skin temperature data using either items of portable equipment (like smartphones) or wearables (such as fitness trackers, earbuds, or smart watches) has numerous tangible benefits. It can potentially provide early indications of infection as well as uncovering underlying health conditions. Furthermore, if carried out regularly throughout the day, temperature measurements could help with fertility tracking, stress monitoring and analysis of circadian rhythms (so sleep patterns can be improved). This fits in with the growing popularity of wearables—presenting the opportunity for data to be acquired on a continuous basis (or at least for a large proportion of the time) as the person will already be wearing such technology for another purpose.

Different approaches to temperature measurement

Two basic methodologies exist for gaining temperature data. These rely on contact and non-contact arrangements. Thermometry based on direct contact is prone to inaccuracies due to difficulties keeping a stable, good quality thermal interface connection between the sensor and the subject's skin. If the sensor is not in proper thermal contact with the skin, then the data quality derived will be poor.

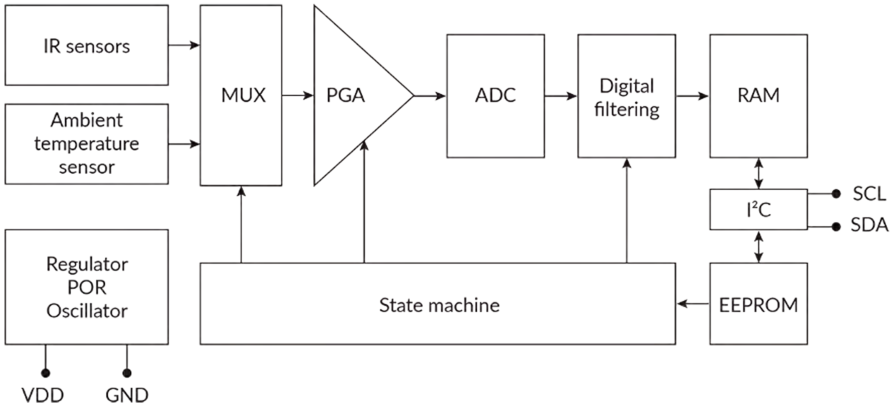
In contrast, non-contact temperature measurement does not experience that problem. Here, energy emitted from the target object at far-infrared (FIR) frequencies (in the 2µm to 14µm wavelength region) is detected. From this, the actual temperature of the target object can be calculated. When dealing specifically with human thermometry, there are places on the body (referred to as proximal points) where skin temperature can be correlated to core body temperature.

Proximal temperature measurement points include the forehead, the corner of the eye next to the nose, inside the ear, and behind the ear. If non-contact measurement is performed at these points, then core temperature extrapolation is possible.

Applying temperature measurement to wearables and smartphones

Key engineering challenges must be overcome if skin thermometry is to be used in a wearable/portable

The MLX90632 temperature sensor from Melexis



Functional block diagram for the MLX90632

equipment context. First, temperature sensing devices must be small enough to fit into electronic designs that have acute size constraints without compromising performance. Second, these devices' power consumption figures need to be kept as low as possible, so equipment battery life is not shortened by their use.

An issue that sensor miniaturization brings with it is that, as devices get smaller, it becomes more difficult to maintain their thermal stability, which consequently impacts on their accuracy levels. Generally, FIR temperature sensor accuracy is influenced by thermal gradients caused by other sources of heat within the vicinity. Unfortunately, smaller sensor packaging only makes matters worse, with devices being more seriously affected.

It must also be recognized that integration into wearables/portable equipment is likely to have detrimental thermal implications too. For example, due to there being very limited board space available, the temperature sensing device might end up being placed close to a microprocessor that is generating relatively large amounts of heat. Effective mechanisms are needed to compensate for the presence of unwanted parasitic signals caused by external heat sources, otherwise acquired temperature data will not be of real value. Greater thermal stability can be attained through placing sensor elements within large metal can packages. These offer substantial thermal mass and elevated thermal conductivity properties. However, arrangements of that kind will clearly not work in system designs where space is limited.

By carrying out extensive modeling and characterization work across a multitude of different scenarios, then applying sophisticated compensation algorithms, the outputs from compact FIR sensors can be augmented. The upshot is significant signal thermal stability improvements.

Compact, thermally-stable, and power-efficient non-contact thermometry

The engineering team at Melexis appreciated from an early stage that inclusion of non-contact measurement in consumer electronic products would become increasingly commonplace. This was the motivation behind the development of the MLX90632, which is already being incorporated into smart watches and smartphone handsets from several of the world's most high-profile consumer technology brands.

This factory-calibrated FIR sensor device features advanced MEMS thermopile technology. Dedicated active compensation algorithms safeguard against the effects of external thermal disturbances. Once temperature measurements have been taken by the thermopile, the signal is amplified, translated into digital form, and then filtered. The device's I2C bus permits subsequent interfacing with the system microcontroller unit (MCU).

Commercial and medical grade versions of the MLX90632 are available, with the medical grade version delivering ±0.2°C accuracy over object temperatures spanning from 35°C to 42°C (meaning that the human body temperature range is fully covered). This accuracy satisfies both FDA and CE medical equipment guidelines.

A simple-to-use software driver allows the duty cycle to be set as power budget requirements dictate. For example, at a rate of one measurement per minute, the MLX90632 draws only 100µW. Compactness is another advantage, with the surface-mount devices housed in QFN packages (dimensions being just 3mm x 3mm x 1mm).

As the MLX90632 relies on FIR (2µm to 14µm) operation, there is no possibility of near-infrared (NIR) emissions interfering with the results obtained. For instance, it may be that equipment is simultaneously taking photo-plethysmography (PPG) measurements (for heart rate monitoring) using NIR in the 600nm-900nm range, but this does not pose a problem.

Conclusion

Accurate temperature measurement is a desirable function that will drive wearable/portable hardware sales; however, exacting operational demands must be met. A thermometry solution that combines medical-grade accuracy, compact form factor, and assured thermal stability is thus mandated. The latest sensor innovations are making this a reality. Not only are these devices opening up new prospects in the consumer electronics sector, but they are also highly suited to use in clinical thermometry and diagnostic tools.

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