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TRENDS SHAPING MILITARY CONNECTOR PRODUCT DEVELOPMENT - PAGE 08

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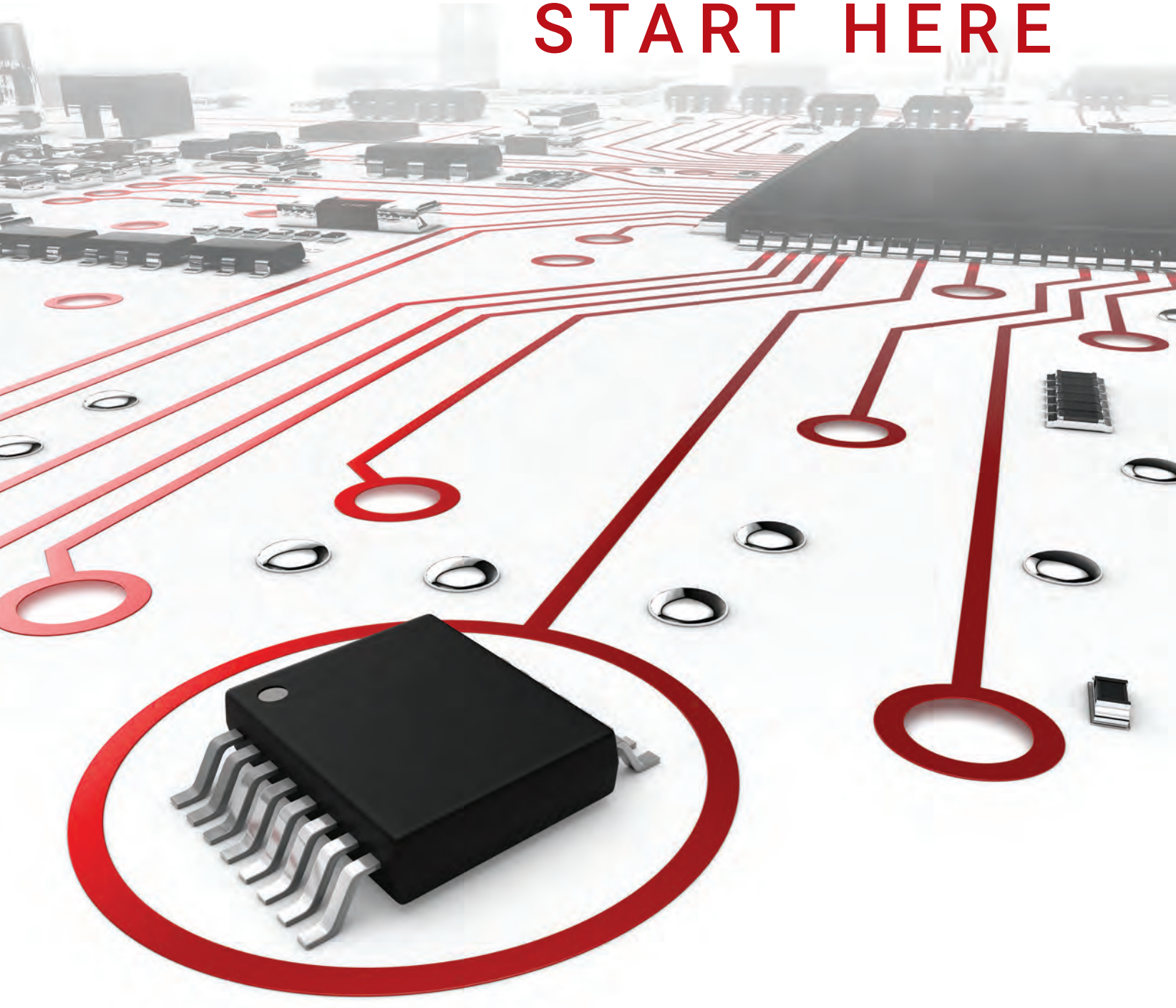

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EDITORS WORD

Close, but no cigar (yet)

Things are starting to move quickly on the artificial intelligence (AI) front with respect to electronic design. On the hardware side, creators of the electronic design automation (EDA) tools employed to develop silicon chips and electronic systems are starting to incorporate AI into their design and verification applications.

Similarly, when it comes to software, developers have started using AI in the form of tools like Copilot. As the developer enters comments or code into their editor, Copilot interactively offers suggestions for its own comments and code. Current market studies indicate that Copilot accounts for around 60% of newly developed code and that developers are spending approximately 55% less time writing new code.

This all sounds wonderful (you may be thinking "increased productivity") until we learn that about 40% of the code generated by Copilot contains logical bugs and security vulnerabilities (this is largely since it's been trained on open-source code that itself contains bugs). Programmers typically spend 20% of their time thinking about the code they are going to write, 30% of their time writing the code they just thought about, and 50% of their time debugging the code they've just written. Now, with Copilot, they can create buggy code quicker (woo-hoo).

But turn that frown upside down into a smile because a company called Metabob recently introduced a new AI that can scrutinize both human and AI-generated code, detect problems, and suggest solutions. We truly do live in interesting times.

Max Maxfield

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Editor, DENA

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ecia Connect. Influence. Optimize

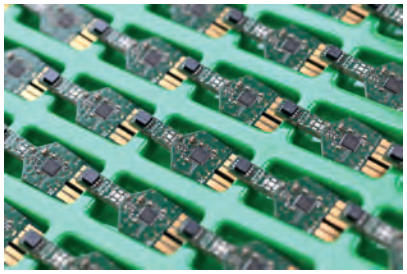
TOP STORY

IAR elevates code security

IAR, the global leader in embedded software and services, is pleased to announce v9.40 of the IAR Embedded Workbench for Arm. This latest update introduces an advancement in code security: the integration of the pointer Authentication and Branch Target Identification (PACBTI) extension for Armv8.1-M. With PACBTI, user applications gain protection through the implementation of cryptographic signatures, effectively preventing attackers from taking control of the entire system. The release also features enhanced smart IDE Build Actions, elevating the development experience for software engineers.

Driven by growing demands for safety products due to legislation and regulation, IAR's latest release addresses the critical need for enhanced code security. Among the notable highlights, the new compiler functions within the IAR Embedded Workbench for Arm complemented by the PACBTI extension and provides a robust defense against two prevalent security exploits: Return-Oriented Programming (ROP) and Jump-Oriented Programming (JOP). Both these techniques involve leveraging existing code segments within the user application. By gaining control of the call stack through methods like stack smashing, attackers overwrite crucial pointers stored in the stack to point, redirecting them towards identified vulnerable code snippets that serve the attacker's purposes. With the inclusion of these new functions, IAR Embedded Workbench establishes formidable barriers, making it significantly more challenging for attackers to exploit code and compromise system integrity.

www.iar.com



Flusso launches four gas flow sensor modules

Flusso has announced a range of 'plug and play' gas flow sensor electronics (FSE) modules to help companies more easily and quickly integrate flow and temperature measurement features into their new product designs.

The four new modules are based on two of Flusso's existing gas flow sensor product lines: the FLS122, launched last year as the world's smallest air velocity sensor with a footprint of 3.5 mm x 3.5 mm, and the FLS11X series of gas flow and differential pressure (DP) sensors. Both sensor families use a unique configuration of four temperature sensing elements on a CMOS MEMS die to offer accurate real-time flow and temperature measurements. These new modules provide a digital numerical output via I2C for easy system integration and communication within new or existing product designs.

www.flussoltd.com

ACEINNA announces IMU for autonomous vehicles

ACEINNA has announced the general availability of the IMU330RA high performance inertial measurement unit (IMU). The IMU330RA is an easy-to-integrate, high-performance 6-DOF inertial sensor packaged in a ruggedized, sealed over-molded plastic housing at IP69K level. This IMU features a redundant 3-Axis Accelerometer and 3-Axis Rate Gyroscope sensors for excellent accuracy and reliability.

The module supports both 1000Base-T1 Automotive Ethernet and CAN-FD interfaces, providing up to 1000Hz update rate with low latency. The IMU330RA is an automotive grade, ASIL B certified device, which serves as the basis for customer positioning system integration to ASIL D.

www.aceinna.com

A novel concept in circuit protection for avionics

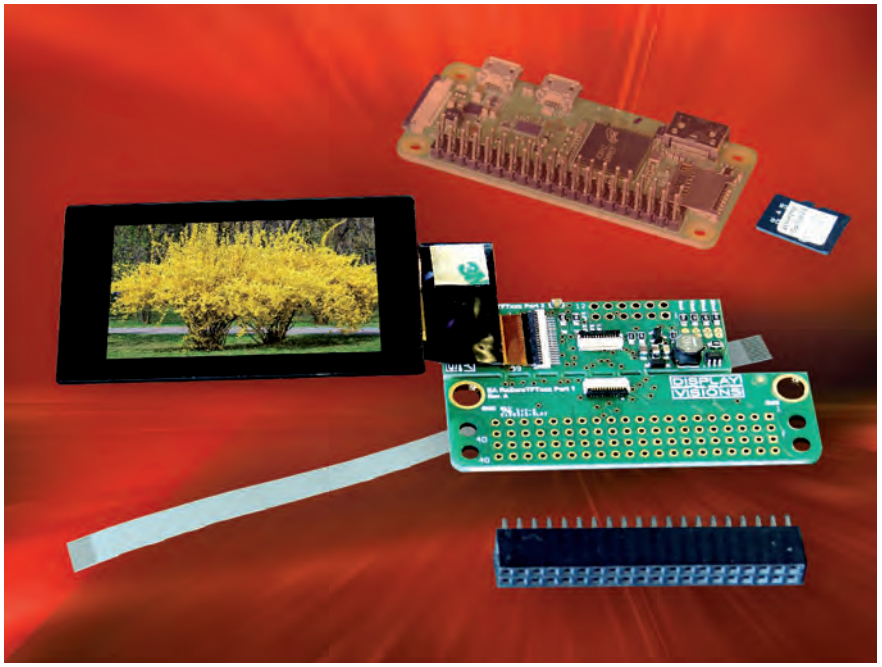
SCHURTER has introduced the FRM-A panel mount fuse holder with DRM-A SMT fuse: a small, light, and robust circuit protection solution designed for avionics applications. The extreme-performance circuit protection system is

the most compact in its class, measuring <15mm deep behind the panel.

The ultra-compact FRM-A fuse holder is originally designed to withstand harsh environmental conditions in the avionics industry, qualified for use up to 50,000 feet. However, its modest dimensions and high ingress protection rating of IP67 make it ideal for use in any challenging environment. The DRM-A is a fast-acting ceramic SMT fuse built according to UL 248-14. It uses gold plating on the endcaps to prevent tin whiskers. It was designed, developed, and explicitly qualified for avionics applications.

Used together or the fuse separately, the FRM-A and DRM-A have a broad range of application use in industrial markets, AV/IT applications according to IEC/UL 62368-1, as well as household appliances according to IEC 60335-1.

www.schurter.com



IPS displays on Raspberry Pi Zero

DISPLAY VISIONS allows for easy connection of small displays from 1.5” directly to the Raspberry Pi Zero and the Raspberry Pi Zero 2. All monitor outputs from the small computer are automatically redirected to a high-quality industrial grade IPS display. Linux is used as an operating system.

As a result, individual, compact applications are able to produce output on a small color display. Furthermore, inputs are possible, including a touch panel integrated into the display. The programming language for applications is Python or C, as is typical for Raspberry.

To make it easy to get started, DISPLAY VISIONS offers a RaZeroTFT starter package. This consists of an interface board and a suitable 1.5”, 2”, 2.8”, or 3.5” display. The displays are equipped with a capacitive touch panel (with the exception of the smallest display). At 1,000 cd/m², these displays are extremely bright and easy to read, even in sunlight. Thanks to IPS technology, they provide brilliant colors in all viewing directions. All displays can be installed horizontally or vertically.

www.arkco-sales.com

OKW’s new SOLID-BOX plastic enclosures for industrial electronics

OKW has launched robust new SOLID-BOX plastic enclosures for desktop and wall-mount electronics used in challenging industrial and outdoor locations. With IK 08 impact protection, these IP 66/IP 67 sealed enclosures are ideal for a wide range of applications including plant and machine construction, HVAC, IoT/IIoT, smart factory/ Industry 4.0, gateways, data loggers, ICT, electrical installations, measurement and control, agriculture and farming, sensor systems and safety engineering.

SOLID-BOX has a smart, highly polished finish. Flush-fitting snap-on trims conceal the tamperproof and corrosion-resistant Torx lid and fixing screws. The lid screws are captive. All the fixings are situated outside the sealed interior. Screw channels under the trims enable direct, concealed wall mounting. The enclosures can be installed ‘lid closed’—protecting the seal and electronics.

A generous recess on the slightly bevelled lid can accommodate a large membrane keypad or product label, while the bottom section has two deeply recessed areas to protect connectors, switches and other interfaces. Inside, there are fastening pillars for PCBs, DIN rails and mounting plates.

www.okwenclosures.com

New microwave switch design tool from Pickering Interfaces

Pickering Interfaces recently announced its Microwave Switch Design Tool, a new free online tool for configuring flexible LXI microwave switching products. The dedicated tool will simplify the configuration of custom LXI RF & microwave switching systems, helping bring powerful, flexible microwave design functionality to customers building systems for signal routing applications across 5G, wireless & telecommunications, semiconductor, medical, and aerospace and defense.

Using the interactive online tool, engineers can specify and configure a mix of high-performance microwave LXI relays, up to 110GHz bandwidth, with 50Ω or 75Ω impedance, and a range of connector types – including the location of individual microwave switching elements through to the associated labeling requirements. Their LXI microwave switch platform design can generate a complete system quotation and unique part number that can be ordered directly from Pickering Interfaces, where it will be built and delivered as a custom system.

www.pickeringtest.com

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Trends shaping military connector product development

In addition to SWaP, four additional trends influence modern military connector design

Gia Hayes, VP, Mil/ Aero Segment, TTI

In the high-intensity world of military operations, the technologies that support the troops are essential to deliver performance and safety when it matters most. Even the smallest components—like connectors—can play a pivotal role in ensuring the equipment operates at its peak performance.

Two well-known standards describing military interconnector size, weight, and power (SWaP) specifications help to standardize the designs to simplify the system connection. They are MIL-DTL-83513 (micro-D connectors) and MIL-DTL-32139 (nano-miniature connectors). The exact SWaP parameters vary based on the number and arrangement of pin connections and the housing in a manufacturer's specific design. The standard also calls out the orientation of the connector, such as straight, 90° angle, PCB mount, or other styles.

The standards limit the current load to ~3A max per contact and can have up to 100 pins per configuration, though exact guidance considers these standards in concert with connector design guidance. And, while SWaP values are the more well-known, four additional advanced trends influence modern military connector design.

Enhanced Durability

Military applications present engineers with a durability challenge. Existing connectors can withstand harsh environments such as subsea and high salt spray concentrations (to comply with the appropriate MIL Specs). However, customers developing new aerospace applications assume total reliability and require durability beyond the existing levels covered in the standard.

An example of the increased durability requirements could come from a manufacturer looking for high-impact connectors that can withstand ten shuttle launches. The company also expects the connectors to be repurposed if supporting components can be reused, which is increasingly common for expensive spacecraft launches. In addition, connectors that do not require replacement at each launch offer substantial cost savings (with a quick payback of any additional capital cost) while improving durability.

Ruggedness: The term "rugged" is related to durability by conveying an item's resistance to increasingly harsh environments. A current trend is to design sealed connectors into flight controls and landing gear systems. The connectors are easier to install and can endure the stresses of flight to add ruggedness to the assemblies.

Other design conditions for new military connectors include:

- Temperature exposure from –150°C to +150°C
- Environments containing dust, dirt, water, chemicals, corrosion from atomic oxygen exposure
- A range of ambient pressures
- Thermal cycling
- Thermal shock
- Shock exposures up to 300g/load

Signal integrity and EMI/RFI protection

Signal integrity is essential for high-speed military

applications operating in rugged environments. Electromagnetic interference (EMI) and radio frequency interference (RFI) can introduce noise and other disturbances into the signal path. These inefficiencies erode the signal strength, compromising the signal and reducing the connectors' reliability and response time. In addition, EMI and RFI can also have the secondary effect of radiation emissions, which further compromises component performance.

Fortunately, engineers can design in several control measures to address these interference types. The first two control levers are MIL-STD-461 standard compliance and proper signal integrity design. The standard ensures that the connectors should work in their appropriate conditions, while the design practices limit signal crosstalk and reflection that degrade the signal.

Designers can also add shielding, filtering, and grounding to control and direct harmful interference away from the signal to preserve its quality.

Reduced package size and miniaturization

Miniaturization is an enduring trend in nearly all electronics (historically following Moore's Law, which describes a continual increase in computing density). Along with transistor dimensions decreasing from millimeters in the 1940s to tens of nanometers in the 2020s, thereby enabling miniaturized components, the shift from analog to digital has had compounded positive effects on military connectors.

Increased processing density enables a smaller packaging envelope for the connectors. This advantage releases critical design space for additional design flexibility, saving materials and costs. In addition, smaller sizes can be lighter weight and may have fewer losses due to shorter run paths.

High-speed and high-bandwidth

Modern military operations need technology to respond in real time. As a result, many applications require speeds up to 10Gb/s, with the requirement (either stated or implied) of maintaining reliability. As a result, engineers are adding networking connectors into commercial and military/aerospace avionics designs. These connectors will enable the technology to realize the advantages of 5G for rapid, high-quality, high-volume data transmission.

Fiber Optics: A recent design engineering interest in delivering high-speed and bandwidth military connectors uses fiber optics. These fibers enable efficient, safe, and accurate missile firing from air, land, or sea launch points. Following standards MIL-DTL-38999, 28876, and others, these cables can transmit large amounts of data over long distances with minimal loss of reliability and consistent, high-accuracy performance.

Fiber optics are ideal in several areas. First, they are spatially efficient, enabling smaller package sizes than traditional copper wire, thereby creating redundancy opportunities for increased system resiliency or retrofitting into existing systems to avoid capital expense.

Takeaways

Military applications expose connectors to some of the harshest environments on Earth. Protecting and ensuring connector performance is vital to the success, safety, security, and outcomes of military operations. Engineers are prepared for these challenges, augmenting the current size, weight, and power guidance with enhanced design features.

"Protecting and ensuring connector performance is vital to the success, safety, security, and outcomes of military operations"

Boosting durability, signal integrity through interference mitigation, miniaturization to reduce package size, and fiber optics for high-speed and high bandwidth are four approaches that can address rugged environment challenges head-on. Adding these features to connector designs ensures that critical military applications will perform at peak levels when they are needed the most.

www.tti.com

Harwin adds female contact to its Datamate Mix-Tek option

New M80-310 contacts can be used with the complete range of Mix-Tek Hi-Rel housing types

Harwin is a globally recognized leader in high-reliability (Hi-Rel) interconnect solutions. Capable of dealing with the most challenging of application demands, Harwin's connectors are pivotal in modern avionics, defense, space, medical, industrial, oil and gas, and motorsport systems.

For almost 70 years, the company has been setting new benchmarks in terms of innovation. Harwin's engineering team has developed an unmatched array of Hi-Rel products that outperform the competition. Among these are the Gecko, Datamate, Mix-Tek, and M300 product lines.

Building on its program where the different elements of its 4mm-pitch Datamate Mix-Tek connectors can be sourced separately, Harwin now offers a new female contact option to its customer base. Like all Mix-Tek coax contacts, the M80-310 is designed for data carrying, with support for frequencies reaching up to 6GHz. This latest contact can be fitted with a 1.19mm/0.047-inch diameter semi-rigid coaxial cable. The 90° orientation means that it is optimized for situations where there is limited room available above a cable-to-board connection.

These new M80-310 contacts are suitable for use with the complete range of different Mix-Tek Hi-Rel housing types—from 2 to 12 position versions. These housings come with a variety of jackscrew styles to ensure mated connections capable of resisting up to 10G vibration and 100G shock. They are also fully compatible with all existing male coax contacts in the Mix-Tek portfolio, giving a 50Ω impedance connection. With gold plated contacts and outer shell, these contacts can withstand a minimum of 500 mating cycles. These contacts will be stocked and available through Harwin's global distribution network. Among the main applications that they will be integrated into are robots, industrial equipment, military/aerospace hardware, and satellites/CubeSats.

"Based on numerous customer enquiries recently received, we could see that there was a real need for a Datamate Mix-Tek contact variant that would support 0.047-inch semi-rigid coaxial," states John Brunt, Product Manager for Datamate at Harwin. "This particular cabling format is proving very popular in a variety of industry sectors, addressing scenarios where built-in shielding and tight routing are required."

www.harwin.com

Assuring GaN security of supply

Performance and reliability come as standard with Innoscience

Gallium nitride (GaN) is now widely used in a variety of applications, including chargers and adapters for mobile phones where it delivers efficiency and power density benefits, as well as in other sectors such as automotive, data centers, LED drivers, renewable energy, consumer, audio and phone handsets, for example. Engineers have realised that GaN's superior switching performance is suitable for countless applications, and they are growing increasingly confident in the ability of suppliers like Innoscience to deliver proven technology combined with rugged and qualified processes—not to mention massive capacity.

Innoscience is the world's largest manufacturing company fully focused on 8-inch GaN-on-Si technology. From the very beginning, Innoscience management understood that, for GaN technology to become ubiquitous in many markets, performance and reliability—whilst vital considerations—were only a starting point.

Before GaN could become widely adopted, customers would have three additional key demands. First, that GaN technology devices must be affordable as the industry isn't willing to pay a big premium. Second, a large manufacturing capacity is necessary in order to deliver large volumes and absorb demand fluctuations. And third, customers require security of supply, allowing them to develop their products and systems using new GaN devices safe in the knowledge there won't be production discontinuations and shortages.

Innoscience executives understood that only by focusing on 8-inch GaN-on-Si technology, by dramatically scaling-up GaN-on-Si device manufacturing, and by controlling its own production fabs would it be possible to meet the requirements of the electronic industry (namely: price, volume, and security of supply).

Innovative technology

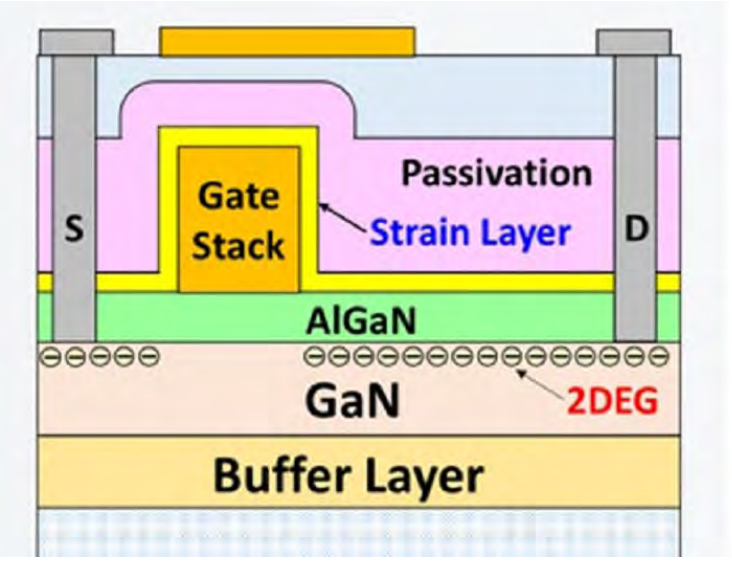
Let's look at the technology Innoscience has developed together with its trusted international partners. Power semiconductor engineers demand devices that show a normally-off operation; i.e., no current conduction when the transistor's gate is set at 0V. Since the natural form of GaN HEMTs (High Electron Mobility Transistors) is normally-on (so-called depletion mode), special drivers must be placed in cascode package solutions to realize normally-off operation.

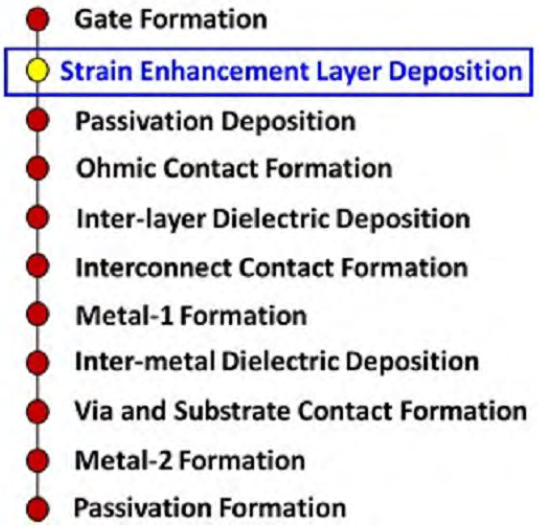
However, Innoscience's GaN HEMTs are intrinsically normally-off (enhancement mode) devices. Normally-off operation is realized by growing a p-GaN layer on top of the AlGaN barrier, forming a Schottky contact with the p-GaN layer. This increases the potential in the channel at the equilibrium, resulting in normally-off/e-mode operation.

Low specific $R_{DS(on)}$

A key parameter for defining device performance is the specific $R_{DS(on)}$, the on-resistance per unit area. The lower the specific $R_{DS(on)}$, the smaller a device can be made, enabling more devices per wafer and lower device cost.

Innoscience developed a proprietary strain





Innoscience has developed a strain enhancement layer technology resulting in low $R_{DS(on)}$

enhancement layer technology, which consists of the deposition of a specific layer after the gate stack definition. The stress modulation created by the strain enhancement layer induces additional piezoelectric polarizations, which cause the 2DEG density to increase reducing the sheet resistance by 66%. Since the strain enhancement layer is deposited after the gate formation, it affects the resistance only in the access region and it does not impact other device parameters such as threshold and leakage, etc.

Therefore, Innoscience's GaN-on-Si e-mode HEMTs show very low specific on-resistance. Because Innoscience has optimized both epitaxy as well as device process technology, the (dynamic) $R_{DS(on)}$ does not increase over the full temperature and voltage range, suiting it for power switching applications.

Today, Innoscience can produce more than 10,000 8-inch GaN-on-Si wafers every month; this will increase to 70,000 wafers per month by 2025. The first Innoscience fab is already qualified to ISO9001 and the IATF 16949:2016 certification for automotive use. These GaN HEMTs are also qualified to the JEDEC standard as Innoscience performs more advanced reliability tests to verity its devices.

Conclusion

Uniquely for a GaN company, Innoscience offers devices that cover the low voltage (30-150V) and high voltage (650V) range. Innoscience's GaN HEMTs (InnoGaN) are available from 30-150V in chip scale packages (CSPs) measuring 2x2mm to 2.2x3.2mm with $R_{DS(on)}$ as low as 5.5mΩ (typical). Furthermore, 650V parts in DFN and wafer scale feature $R_{DS(on)}$ levels as low as 106mΩ (typical). Innoscience GaN HEMTs are being used in USB-PD chargers up to 120W and in LLC converters. They are also to be found inside data center power supply racks.

By combining world-class technology, state-of-the-art processing technology, and the world's largest 8-inch GaN-on-Si capacity, Innoscience is answering both engineering and commercial challenges, enabling designers working in all market sectors to benefit from proven performance benefits with no cost penalty.

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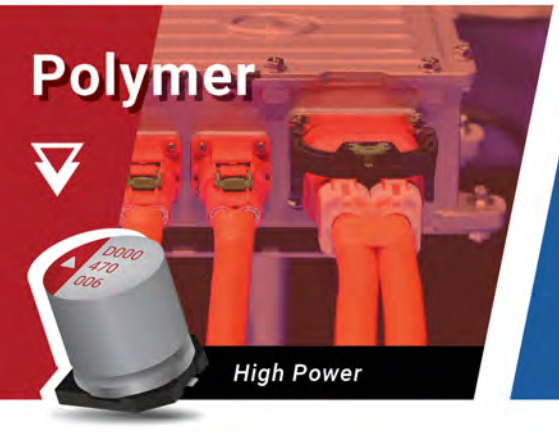

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Tantalum polymer capacitors in aerospace applications

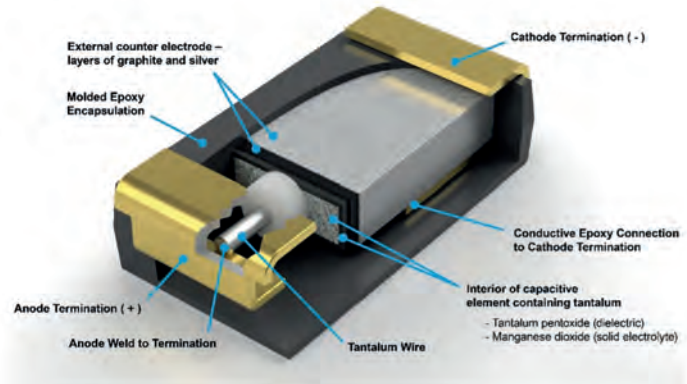
These devices provide an added design option for next-generation aerospace applications

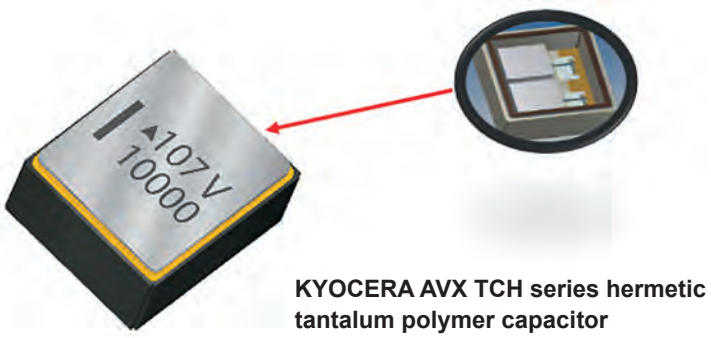
Aerospace is becoming an increasingly active marketplace, especially the overall satellite sector with market growth projections increasing from ~$6 billion USD in 2023 to $9.6 billion USD by 2030 (Grandview Research). Whether it be low-earth orbit (LEO), medium-earth orbit (MEO), or high earth orbit (HEO), the advances in satellite performance have been driven by active electronic components such as microcontrollers, FPGAs, and processing cores. With the rapid and continuous progression of ICs (integrated circuits), the limiting factor to system performance is the passive components surrounding them.

Power management innovations have played a critical role in these advancements as the complexity of the ICs becomes more prevalent. To add to the complexity, the power quality must also be consistent when raw power is obtained from solar panels or batteries. Size and weight, as in all aerospace applications, play a massive role in deciding which components will go into the circuitry of satellites. Solid tantalum capacitors have been used as bulk capacitors in aerospace applications for the past two decades with extremely positive results. However, to keep up with the higher voltage stability and capacitance ranges of next-generation ICs, the implementation of tantalum polymer capacitors is a welcomed added design option.

Tantalum polymers offer reduced equivalent series resistance (ESR) and, therefore, higher RMS current capability associated with cutting-edge flight platforms. Both tantalum capacitor technologies will be utilized in next-generation advanced flight platforms in areas where they individually excel regardless of orbit characteristics.

KYOCERA AVX TCS series molded tantalum polymer capacitor





KYOCERA AVX TCH series hermetic tantalum polymer capacitor

Within the satellite/aerospace marketplace, there are two main business sectors: military and commercial. The former are expected to need high-reliability tantalum and hermetically sealed tantalum polymer capacitors, while the latter will most likely go for the molded options for cost-restrained and quick-turn designs. There is a space and military performance standard being created, MIL-PRF-32700, for tantalum polymer capacitors, indicating interest in documented reliability from end customers.

The construction of hermetic tantalum capacitors should be reviewed given recent agency interest, testing and flight acceptance. Hermetic tantalum polymers use polymer cathodes, which are moisture sensitive, but this sensitivity is eliminated by encapsulating the anode in a hermetic package filled with an inert gas. An example of a hermetic tantalum polymer option is the KYOCERA AVX TCH series.

Molded tantalum polymer capacitors also exist, and their performance has been greatly improved by rigorous testing and modernized engineering processes. This work has pinpointed moisture ingress areas and resulted in the addition of moisture barriers to create a molded package that is as close to hermetic as possible while reducing the cost associated with wholly hermetic options. An example of the molded option is the KYOCERA AVX TCS series. Conductive polymer stability throughout thermal cycling and low ESR makes them an ideal choice for high-power filtering. High altitude, low/high pressure, vacuum, and radiation have minimal impact on the functionality of conductive polymer capacitors, making them ideal solutions for aerospace applications.

Mesh satellites, swarm satellites, cube satellites, telecommunication satellites, and reconnaissance satellites are all just the tip of the iceberg when it comes to next-generation aerospace technology. With the active electronics contained in these satellites constantly pushing the boundaries of existing passive components, there will be a huge demand for small, lightweight, reliable bulk capacitors. Tantalum polymer devices like the ones discussed here are an example that the passive components industry is aware of—and proactively providing solutions for—commercial to mission-critical space and flight applications.

www.kyocera-avx.com

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Delving into the world of analog IP for ICs

Why are the analog and digital portions of an IC design so different?

Since the creation of the first transistor, the complexity of integrated circuit (IC) design has increased massively, reflecting the renowned "Moore's Law" of semiconductor production. Developments in digital design have been a key contributor to this constant expansion. What many people don't realize is that even in the case of "purely digital" IC designs, such as predominantly digital system-on-chip (SoC) devices, there are going to be some analog elements (e.g., temperature, voltage, and process sensors along with corresponding analog-to-digital converters). How do the digital and analog portions of the design differ? How does analog IP work? And does "silicon-proven" analog IP really mean high-quality IP?

Contemporary digital design

Digital design is initially carried out in a mostly process agnostic manner, with the achievable performance and the likelihood of logic depth serving as major guiding factors. Ease of design portability between process nodes is therefore viable without compromising the verification quality. As the level of design capture abstraction has increased, a thorough design tool flow and verification methodology to evaluate consistency and compliance at each stage of the flow has led to a significant improvement in designer productivity. Together with upgraded verification and signoff tools, this has made it possible to automate the digital design process to produce complex, high-quality ICs that no longer rely on silicon validation for proof.

Even though the digital design is process independent, the deployment of the design from synthesis through place-and-route takes account of the target process node through the various models and signoff procedures. The same design can, in effect, be implemented significantly differently and optimized to benefit from the specific process features.

Digital vs. analog design

There are some parallels between the analog design flow and the digital design flow—for instance, the analog flow's "architecture" and the digital flow's "functional design" are similar, as are the analog flow's "layout" and digital flow's "place-and-route." However, there are also clear differences between the two.

First, unlike the "linear" digital design flow, the analog design flow involves circular iterations across multiple cycles. The design flow will iterate several times in the analog design flow loop, often between the layout and post-sim stages. This depends on the complexity of the analog circuit block, the circuit designer's experience, knowledge of the technology node, and many other considerations. In some circumstances, the architecture chosen cannot fulfil the circuit specifications. This results in a restart from the beginning. The time and effort required to complete an analog circuit are, to put it plainly, approximations. The uncertainty grows as the complexity rises or there are changes in technology.

Chris Morrison, Director of Product Marketing, Agile Analog

Next, the technology or process node of an analog IP is determined at the outset of the design, and the available devices for architecture exploration and design, model cards for simulation, layout rules, and the metal R-C models are all process specific. The entire analog design often needs to be started again from scratch if a project manager decides to select a process node or even adjust the existing node's process options.

Finally, there is very little CAD automation in analog

This table summarizes the key differences between analog and digital design methods, showing why traditional analog design takes more time

	Design Flow	Process	CAD Automation
Digital Design Flow	Linear	Fairly Independent	High
Analog Design Flow	Circular	Highly Dependent	Low

Reuse Risk	Low					High
Process Choice	Identical	Identical	Identical	Identical	Identical	Different
Process Options (e.g. metal stack)	Identical	Different	Identical	Identical	Different	Different
Design parameters	Identical	Identical	Different	Identical	Different	Identical
Functions	Identical	Identical	Identical	Different	Different	Identical
Silicon Proven?	Yes	NO	NO	NO	NO	NO

This table illustrates how process choice, process option, design parameters over corners, and functions are all factors determining the "silicon- proven" validity of the IP

design. Even though there are excellent EDA tools, different analog blocks have different design methods. Also, layout is custom, and simulations are circuit-, process-, and application-dependent.

What makes high-quality analog IP?

The first step is to select a solid circuit architecture that is stable, robust, and suitable for mass production. Up to date process design kits (PDKs) from foundries offer models for the front-end (transistors, varactors, diodes, etc.) and back-end (resistors, capacitors, metals, etc.) for simulations, as well as a variety of command files for DRC, LVS, and parasitic extraction. Today, the major foundries provide PDKs that have very good correlation between model and physical silicon. All that is required is a proper PDK installation and selecting the process option.

Thorough behavioral simulation and circuit simulations at the crucial process, voltage, and temperature (PVT) corners are needed to ensure the circuit will function as expected. Circuit layout involves knowledge of the circuit design and a clear understanding of how the process impacts on analog performance. This requires a skilled group of layout engineers and circuit designers with broad expertise.

With a solid circuit architecture, accurate PDK, thorough simulations, detailed layout, and an experienced team, a high-quality analog IP will be delivered with fewer rounds of iterations. Traditionally, however, analog designers have been hard to find, and high-quality analog IP is expensive.

What is "silicon-proven" IP?

An issue that IC design companies often raise is whether a particular analog IP is "silicon proven" or requiring an analog IP to be "silicon proven" to be qualified for use. The general definition of a "silicon-proven" IP is an IP that has been manufactured on silicon and has had its functionality bench-test measured; hence, verified "on-silicon." Once an IP is "silicon-proven," it gains credibility that it will work as expected on a production chip with the identical layout on the same process technology. However, this silicon proof is based only on a sample as validation of the design is usually measured at specific points.

Whether this "silicon proven" IP is "production quality" is determined before the manufacturing of the IP. This means the architecture chosen, the comprehensive simulations and design corners covered, the diligence put into the layout, and the effort in verification during development. In other words, an IP that is "silicon-proven" is merely a sanity check, only proving that the IP development flow "seems" to be "okay," which really is not sufficient proof of quality.

Some "silicon-proven" IPs come from production chips and have withstood a variety of real-world, high-volume tests. These IPs can be credible in terms of their quality but are designed specifically for a certain product at a particular process node. Process-porting is necessary for a project in a different node, thereby removing the IP from the category of "silicon-proven." It may be possible to modify silicon-tested IPs, but the extra cost ($xxx k) and time (6 months to a year) is likely to be too much to justify. The original IP's "silicon-proven" status is also revoked by modifications.

In summary

Even in predominantly digital ICs, analog design and analog IP have an important role to play. Despite claims about an analog IP being "silicon-proven," the quality of that analog IP is actually determined by the use of a solid architecture, accurate PDK, thorough simulations, and an experienced design team. All these factors are embodied by Agile Analog's innovative analog IP technology.

www.agileanalog.com

"Even in predominantly digital ICs, analog design and analog IP have an important role to play"

Securing the new chiplet era of semiconductor design

SRAM PUFs can form an unclonable identity for every chiplet

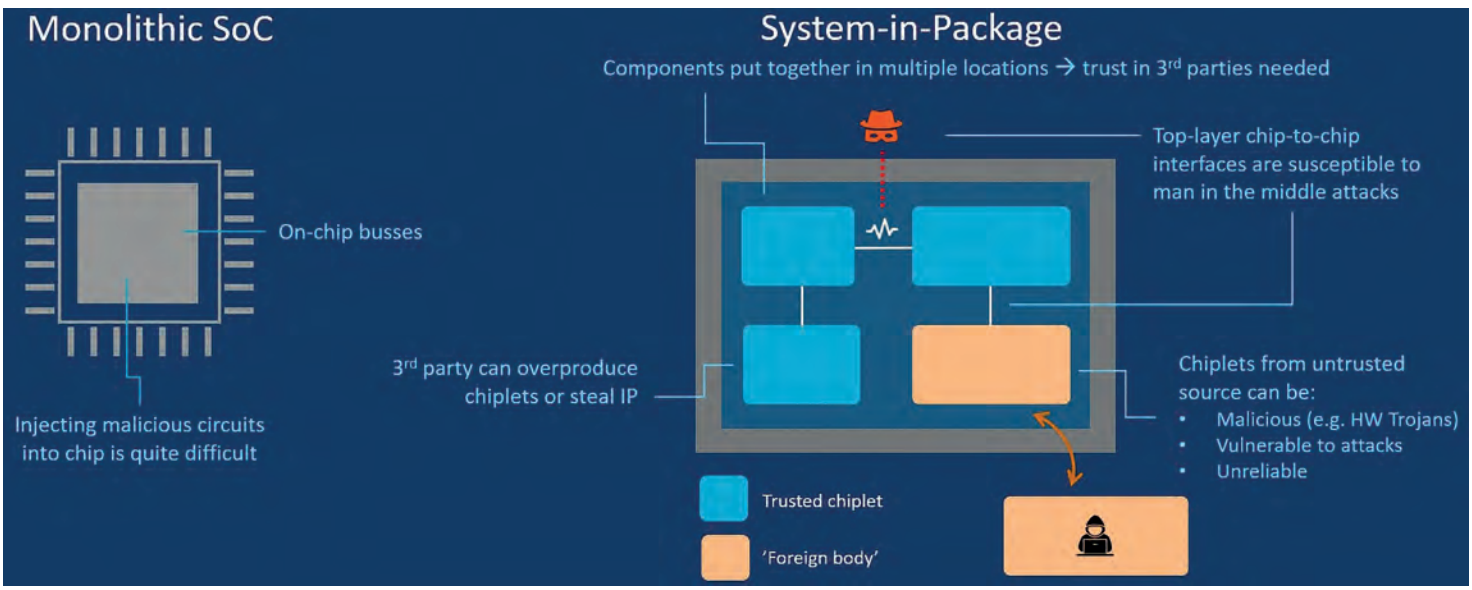
Chip designers are on the frontlines of innovation. Today's advances in consumer electronics, medical devices, and autonomous driving, as well as high-performance computing (HPC), artificial intelligence (AI), and machine learning (ML) systems, all require increasingly complex chip designs.

As chip designs continue to grow more complicated, pushing the limits of Moore's Law, it is becoming increasingly difficult to fit everything onto a single die. This is giving way to a new era in chip design in the form of chiplets, which are smaller, independent semiconductor components that can be combined to create more complex systems.

Chiplets are a new frontier for semiconductor innovation and represent a significant shift in the traditional monolithic approach to chip design and manufacturing. Rather than creating a semiconductor chip as a single, complete die, chiplets offer a modular approach, providing increased flexibility, improved yield, and lower costs. Chiplets can be designed and manufactured separately, then combined on a larger substrate to create a complete system, which is typically called a System-in-Package (SiP). When it comes to manufacturing, chiplets can scale down to new technology nodes easier, resulting in lower costs and faster time to market, while implementing specific functions at their optimal technology node. This is one reason the Gartner Group predicts that, by 2026, 20% of all semiconductor devices shipped will incorporate advanced 3D packaging technology, up from less than 1% in 2021.

Dr. Pim Tuyls, CEO and Founder, Intrinsic-ID

Monolithic vs. System-in-Package (SiP)



Chiplets are rising in popularity because they enable manufacturers to create systems with more features and higher performance without having to design and manufacture all the components on a single chip. This is especially useful for complex systems, enabling applications leveraging artificial intelligence, machine learning, and high-performance computing. Additionally, chiplets can be easily upgraded or replaced in future iterations of the device, thereby allowing for easier maintenance and longer product lifetimes.

The risks of using chiplets

While the use of chiplets represents an exciting new approach to semiconductor design that could help to overcome the limitations of Moore's Law and continue to drive innovation in the computing industry, it doesn't come without risks.

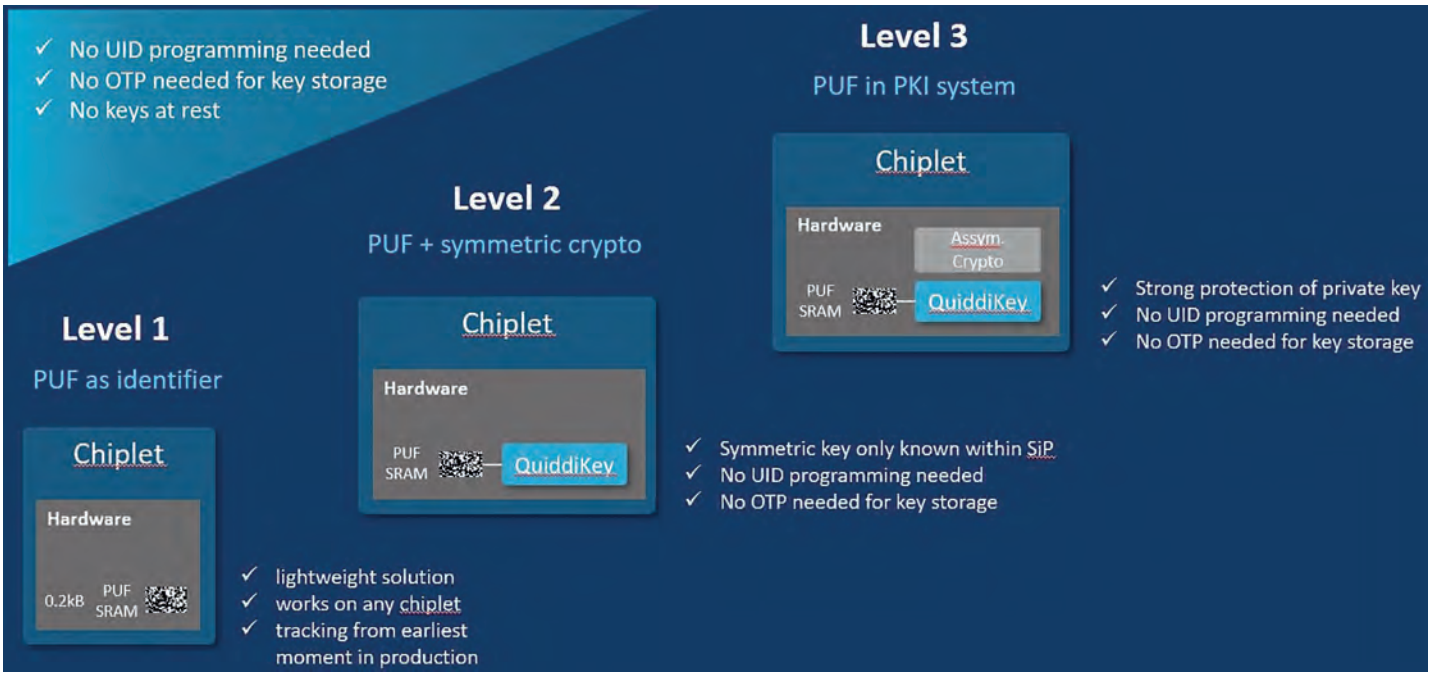
Spreading functionality over multiple chiplets increases security risks. This is because communication between chiplets is easier to eavesdrop and alter than communication on an internal bus inside a single die system-on-chip (SoC) device. Also, different chiplets can be sourced from different vendors and come from different production facilities, which makes the supply chain even more complex and untrustworthy. During manufacturing, chiplets can be used that originate from untrusted manufacturers or, even worse, malicious chiplets can be inserted to serve as Trojan Horses in potential attacks. Finally, with the increasingly complex supply chain, there is also a bigger risk of intellectual property (IP) theft and of chiplets being overproduced by manufacturers.

The good news is that there are ways to ensure every chiplet in a system is genuine, does not come from an untrusted third party, and is sufficiently protected from "man-in-the-middle" attacks that may lead to eavesdropping and alteration of sensitive data. One of these techniques is to use SRAM-based physical unclonable functions (or PUFs) to protect against such security risks.

SRAM PUF technology

Due to deep submicron manufacturing process variations, every transistor has slightly different physical properties. These variations lead to small but measurable differences in terms of electronic properties, such as each transistor's threshold voltage and gain factor. Since these process variations are not fully controllable during manufacturing, these physical device properties cannot be copied or cloned. By utilizing the intrinsic process variations caused by the silicon manufacturing process, PUFs create unique "silicon fingerprints" for every die to serve as identifiers that can then be used to validate the authenticity of each individual chiplet.

The SRAM PUF, which is based on the behavior of standard SRAM memory, is available in almost any digital chiplet. Every SRAM cell has its own



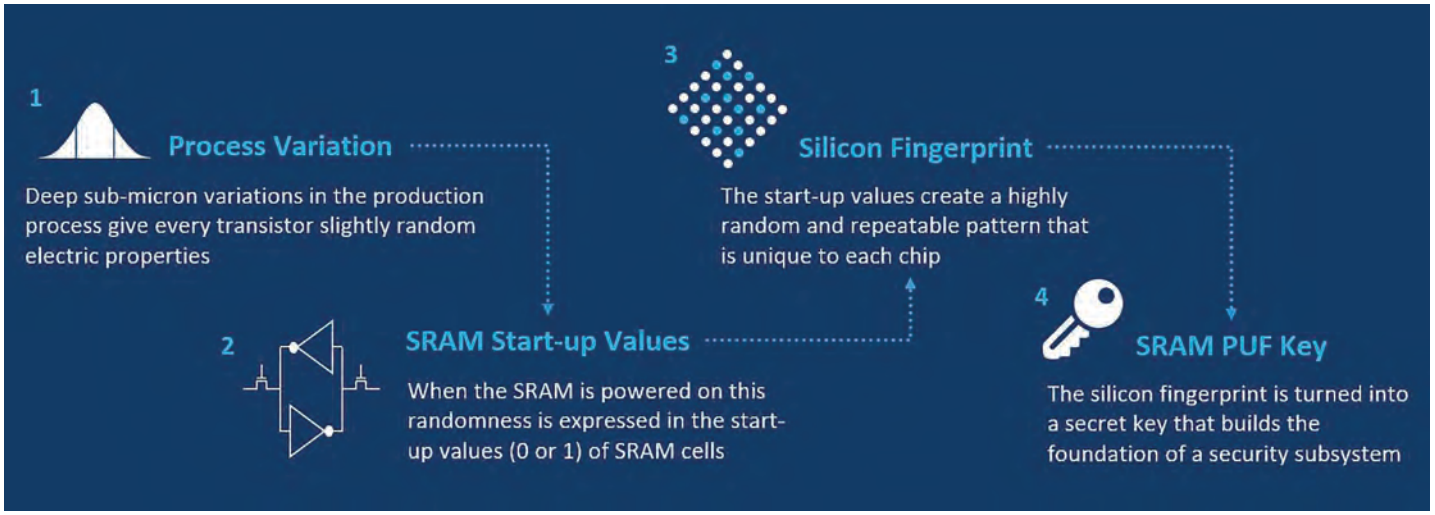
Trust validation levels with PUFs

preferred power-up state resulting from unique local differences in the threshold voltages of its transistors. This uniqueness is captured in a so-called PUF response by reading the power-up values of "uninitialized" SRAM memory. Hence, an SRAM PUF response yields a unique and random pattern of 0s and 1s. This pattern is like a fingerprint for a chiplet since it is unique to a particular SRAM and hence a particular chiplet.

In addition to being used to identify chiplets in the supply chain, these silicon fingerprints can also be turned into a cryptographic key that is unique for the silicon from which it is derived. This root key is reliably reconstructed from the PUF whenever it is needed by the system, without a need for storing it in any form of memory. This means that when the device is powered off, no secret key is present in any form of memory. In effect, the root key is "invisible" to attackers, which makes storage of keys based on PUFs extremely secure.

Combining the availability of this root key with certain cryptographic algorithms allows for communications between individual chiplets to be encrypted, providing security for the complete system. As an added benefit, since the root key is never stored, security can still be guaranteed even if not every individual chiplet contains non-volatile memory (NVM). This is especially important when certain chiplets are produced using advanced technology nodes in which NVM is not always available.

SRAM PUF technology



Enhancing security and trust

A first level of trust validation is obtained by using SRAM PUFs to identify chiplets and detect counterfeit copies. Only a small amount of SRAM on the chiplet is needed to create a fingerprint for that chiplet, and this fingerprint can be stored in a database. Identifying chiplets based on the fingerprints in this database works for any chiplet and enables tracking from the earliest moment in production. This offers a robust and scalable solution, without the need to store an identity or key on the device, enabling the identification and tracking of chiplets that have no NVM available.

A higher level of trust validation (for chiplet and data authentication or for IP binding, for example) can be achieved by extracting cryptographic keys from the PUF and using those keys in combination with symmetric cryptography. A Key Extractor function reliably reconstructs a cryptographic key from an SRAM PUF whenever a key is needed by the system, without a need for storing it in any form of NVM. So, when the device is powered off, no secret keys are present in memory making root keys "invisible" to attackers. Therefore, storage of keys with PUFs adds a layer of security. An additional benefit is that this can also be performed on chiplets that have no NVM available (this scenario is very likely when chiplets are created in advanced technology nodes, where NVM causes scaling issues). This technology can even be retrofitted on existing chiplets. The symmetric crypto algorithms enable the encryption of local data on the chiplet as well as facilitating secure connections, using PUF-based chiplet-unique symmetric keys that are only known within the SiP. Again, this can all be achieved without the need for programming keys or having NVM on the chiplet to store keys.

The strongest level of authentication can be achieved by combining SRAM PUF-based keys with algorithms for asymmetric cryptography that are connected to a traditional public key infrastructure (PKI) system, which is a system used to secure communication and transactions between different entities in a network. In this case, every chiplet obtains a device certificate from the manufacturer guaranteeing its authenticity, which can be verified in a cryptographic authentication protocol by using the manufacturer's public key. A certificate is only as strong as the protection of the private key, so SRAM PUFs are particularly well suited for protecting these keys and therefore the authenticity of the chiplets.

Conclusion

The cryptographic keys extracted from SRAM PUFs can be used to form unclonable identities for every individual chiplet, which allow for identification and authentication of the chiplets throughout the entire supply chain and even in the field. Combining the keys extracted from PUFs with certain cryptographic algorithms allows for encryption of data on chiplets as well as for communications between individual chiplets to be encrypted and authenticated, thereby providing security for the complete system.

Since the root keys are never stored, cannot be altered, and cannot be copied to other chiplets, SRAM PUFs create a hardware root of trust on every individual chiplet. This even works on chiplets produced in advanced technology nodes where NVM is often not an option. Hence, SRAM PUF technology is a valuable tool to ensure our advanced semiconductor designs are created in the most secure and trustworthy way.

www.intrinsic-id.com

"In addition to being used to identify chiplets in the supply chain, PUF-based silicon fingerprints can also be turned into cryptographic keys that are unique for the silicon from which they are derived"

Graphics processors shine in the AI spotlight

CPUs have for long dominated the semiconductor landscape, but GPUs are staging a silent insurrection with the advent of artificial intelligence and piggybacking on this to exponential growth beyond the traditional gaming market.

Manufacturers of graphics processing units (GPUs) are in luck. GPU sales are on the rise and expected to keep increasing, boosted by rocketing demand from a widening range of economic segments, including automotive, electronics, finance, media and entertainment, healthcare, electronics and industrial. Enterprises in all these sectors are hoping to leverage artificial intelligence (AI) to widen their competitive advantages and accelerate innovation and new product development. Over the next decade, the market for graphics processing units (GPUs) is projected to be the hottest segment of the semiconductor industry, according to forecasters who predict the segment will expand at a sizzling 33.5 percent compounded annual growth rate between 2022 and 2030.

If the forecasts, from Reports Insights and other sources, prove accurate, GPU sales may by 2030 represent a whopping 45 percent of the $1 trillion estimated value of the entire semiconductor industry. The researchers estimate sales of GPUs will increase to $450 billion by the end of this decade, from just $44.7 billion, in 2022. This will intensify competition in the segment although observers said they expect Nvidia Corp. to remain the market leader. The company's market share in the total GPU segment, which includes PCs and gaming, is currently estimated at more than 80 percent, with Advanced Micro Devices in second place and Intel Corp. a distant third, according to figures from Jon Peddie Research. New players are crowding into the sector, lured by promises of rapid growth and profitability.

A slowdown in demand for GPUs is not expected anytime soon due to the expansion of interest from new economic segments. Researchers at Spherical Insights said they see the market continuing to grow through 2032, rising to $594.2 billion. AI, cloud and edge computing are driving the market expansion, they said. "The growth is driven by the continuous demand for computing devices, servers, and networking equipment across various industries," said the Spherical Insights analysts, in a statement. "The expansion of emerging technologies, including artificial intelligence, Internet of Things (IoT), and edge computing, further fuels the demand for robust hardware infrastructure. Additionally, the need for reliable hardware components in data centers and the growing adoption of cloud services also contribute to the expected growth of the hardware segment."

GPUs have been around for decades, but they are beginning to attract further interest now as Jon Peddie, a graphics industry veteran and analyst, points out in a newly published book. In the book titled "The History of the GPU – New Developments" Peddie notes that the areas where GPUs are used nowadays have expanded to include "supercomputers, PCs, smartphones and tablets, wearables, game consoles and handhelds, TVs and every type of vehicle." GPUs used to toil in the shadow of central processing units (CPUs), however. Once the more famous rival, CPUs ruled for decades, championed by companies like Intel, which notes on its website that the CPU "is suited to a wide variety of workloads, especially those for which latency or per-core performance are important," adding this "makes it uniquely well equipped for jobs ranging from serial computing to running databases."

But even Intel sees opportunities in the GPU market and is a growing player in the segment. The company regularly unveils new GPU products and is pushing for a bigger role in the AI market. Many of Intel's new GPU products are aimed at the AI market, the company noted in a statement on its website. "Today, GPUs run a growing number of workloads, such as deep learning and artificial intelligence (AI). A GPU or other accelerators are ideal for deep learning training with neural network layers or on massive sets of certain data, like 2D images," Intel noted. "Deep learning algorithms were adapted to use a GPU-accelerated approach. With acceleration, these algorithms gain a significant boost in performance and bring the training time of real-world problems to a feasible and viable range. The combination of CPU and GPU, along with sufficient RAM, offers a great testbed for deep learning and AI."

AI boost

GPUs have invaded even the data center market where CPUs once reigned supreme. In fact, GPUs are suddenly hogging the spotlights, courtesy of the world's huge interest in everything related to artificial intelligence, according to market observers. Once confined to the gaming world, GPUs are increasingly being integrated into other applications. It is now used in many applications as an alternative to CPUs in areas where it can "meet the requirements of demanding computations as well as manage cost savings on hardware and electricity," according to research aggregator Reports Insights. "The growing demand for cross-platform gaming results in the large adoption of GPUs in terms of high computability and performance on various devices and operating systems," the researchers added. "Thus, the current status of GPUs is in terms of continuous advancements and improvements due to regular launches of the latest models by companies such as Nvidia, AMD and Intel."

The race to inject GPUs into AI applications began more than 10 years ago as companies like Nvidia began searching for new ways to gain a bigger share of the semiconductor market. Executives in the industry were trying to raise the prospects for a new form of data processing that they termed "accelerated computing" and which they see helping to loosen Intel Corp.'s hard grip on the processor market. Nvidia called AI the "final frontier" in the computing

world where opportunities in "deep learning" and research simulations could be further explored by researchers and businesses. That frontier was breached years ago when Nvidia began pushing the concept of GPU-accelerated computing, according to company executives.

In a presentation in 2016 at New York University, Jensen Huang, chairman and CEO of Nvidia, explained why he thought GPUs were better suited for advancing the attainment of AI-level programming. "Computer programs contain commands that are largely executed sequentially," Huang said. "Deep learning is a fundamentally new software model where billions of software-neurons and trillions of connections are trained, in parallel. Running DNN [Deep Neural Networks] algorithms and learning from examples, the computer is essentially writing its own software. This radically different software model needs a new computer platform to run efficiently. Accelerated computing is an ideal approach and the GPU is the ideal processor."

While the development work and tests continued, it took several more years for the GPU-centric deep learning to become known to more people than researchers, academicians and general consumers. The explosive introduction last year of ChatGPT and other generative AI-related innovations has now increased awareness of the technology in addition to exposing its utility in areas beyond academia and research. This has also resulted in greater awareness of the role GPU vendors play in the development of the technology and in the management of data centers, according to analysts.

Competition grows

The GPU market first contracted at the beginning of the century when the segment went through a round of consolidation that reduced the number of players. Peddie noted in an earlier book (The History of the GPU – Era and Environment) that the number of suppliers in the segment "peaked" in 1998 although demand for the processors especially in the PC segment continued to rise. AMD and Nvidia led the consolidation of the segment. AMD purchased ATI Technologies Inc. in 2006 and added Xilinx to its list of acquisitions last year. Although Xilinx was not a supplier of GPUs, its FPGA operation complemented AMD's offerings in the area of adaptive computing as CEO Lisa Su said in a statement announcing the closing of the transaction in early 2022.

"The acquisition of Xilinx brings together a highly complementary set of products, customers and markets combined with differentiated IP and world-class talent to create the industry's high-performance and adaptive computing leader," Su said. "Xilinx offers industry-leading FPGAs, adaptive SoCs, AI engines and software expertise that enable AMD to offer the strongest portfolio of high-performance and adaptive computing solutions in the industry and capture a larger share of the approximately $135 billion market opportunity we see across cloud, edge and intelligent devices."

Nvidia too has been active in the M&A market. The company has made more than 20 acquisitions since it was founded in 1993. In 2002, it purchased the intellectual assets of rival graphics chipmaker 3dfx and added Hybrid Graphics in 2006. Its biggest purchase was the $6.9 billion acquisition of Mellanox Technologies, first announced in 2019. The transaction closed in April 2020 and added critical high-performance computing technology to the company's offerings. Many of Nvidia's other acquisitions also brought significant software innovations that were incorporated into its current product portfolio.

"With Mellanox, the new NVIDIA has end-to-end technologies from AI computing to networking, full-stack offerings from processors to software, and significant scale to advance next-generation data centers," said Nvidia's Huang, in a statement announcing the completion of the Mellanox purchase in April 2020. "Our combined expertise, supported by a rich ecosystem of partners, will meet the challenge of surging global demand for consumer internet services, and the application of AI and accelerated data science from cloud to edge to robotics."

The three-horse race of AMD-ATI-Nvidia in the GPU market ended with the purchase of ATI by AMD but other fronts in the GPU war have since opened with Intel now one of the major contenders in the sector. Other companies are also gunning for a share of the market, offering software and IP GPUs, especially for mobile handset applications. Other players include Imagination Technologies and many new entrants from China. The expected growth spurt and high valuation given to Nvidia, which recently crossed the $1 trillion market capitalization level, could result in additional players making efforts to establish a presence in the GPU market, according to Reports Insights.

"The highly competitive market of graphic processors involves established market players such as Intel, Nvidia, AMD, and Intel," the researcher said. "Such market players continuously innovate and expand their market shares through technological advancements due to increased demand for high performance, power efficiency, and increased functionality of GPs. Price competition and shifting consumer preferences are also significant factors that influence the overall market's competitiveness."

Future of GPU

The huge sales growth predicted for GPUs will keep the segment active for a long time and attract new players as well as additional investments from current market players. Demand for GPUs is also expected to remain strong for the foreseeable future due to growing interest from companies that are developing their own deep learning AI accelerators, according to observers. Data center and cloud services companies are also active in this segment and demand for GPUs from these companies will help fuel growth and demand for the processors for years into the future. Demand is also rising from the automotive, industrial and medical markets in addition to the traditional gaming and entertainment segments, sources said.

"These technologies rely on powerful GPUs for processing and rendering graphics, analyzing sensor data, and enabling intelligent decision-making," said Spherical insights, in its report. "The automotive industry's focus on enhancing user experiences, improving safety, and developing autonomous vehicles creates a strong demand for GPUs."

Debug smarter to develop faster

Keep up with faster development cycles by using smarter debugging tools

The level of complexity of embedded devices continues to increase unabated. In my previous column (https://bit.ly/43ENb2W), we considered the use of an adaptation layer, which provides a standard software interface between the various layers of software and hardware forming an embedded device. In this column, we are going to consider the use of debug and test tools to increase efficiency.

Clarinox is a leading provider of software solutions for wireless communication. One of its key offerings is ClariFi, a powerful debugging tool that enables developers to troubleshoot issues in the integration of the ClarinoxBlue and/or ClarinoxWiFi wireless protocol stacks.

Bluetooth and Wi-Fi are ubiquitous wireless technologies that are used in a wide range of devices, including smartphones, laptops, and the large range of electronic devices that wish to interface to things like printers, cameras, and automobiles. ClariFi is designed to make debugging and testing Bluetooth and Wi-Fi issues as efficient as possible.

ClariFi provides a comprehensive set of tools and features that enable developers to quickly identify and resolve issues with the wireless device they are designing. In addition, allowing testing of these devices during various stages of the life cycle of the product. A variety of hardware interface mechanisms can interface to a target product for debugging and testing.

One of the key features of ClariFi is its real-time monitoring capabilities, which allow developers to monitor Bluetooth and Wi-Fi traffic to see exactly what is happening on the wireless network. The ability to do this in real-time makes it much easier to identify issues such as dropped connections, interference, or other anomalies.

ClariFi also provides advanced filtering and search capabilities including script-based pre- and post-processing. Developers can filter the Bluetooth and Wi-Fi traffic based on various criteria, such as the type of packet, the source and destination addresses, or the time stamp. This makes it much easier to isolate specific packets or events that may be causing issues. As these protocols are complex and various vendors are involved for the software and hardware components, ClariF acts as the essential tool for identifying communication between different vendor components to resolve issues.

In addition, ClariFi provides powerful visualization tools, enabling developers to view the Bluetooth and Wi-Fi traffic in various formats, including charts, graphs, and tables. Another key feature of ClariFi is its ability to simulate different network conditions—such as low signal strength or high interference—to see how the Bluetooth or Wi-Fi network performs under these conditions. ClariFi also provides extensive logging and analysis capabilities that allow developers to capture and analyze Bluetooth and Wi-Fi traffic over an extended period, allowing them to identify patterns or trends in the data. Another powerful feature is to allow script-based tests to be injected to the target device for an automated testing infrastructure. This provides an easy way of regression testing after a major software update or automate final product testing to improve product quality.

Trish Messiter, CEO
Clarinox Technologies

Overall, ClariFi is an essential tool for developers working with ClarinoxBlue and/or ClarinoxWiFi software. It provides a comprehensive set of features and tools that enable developers to quickly identify and resolve issues with these wireless technologies. Its real-time monitoring capabilities, advanced filtering and search capabilities, powerful visualization tools, simulation capabilities, and extensive logging and analysis capabilities make it an indispensable tool for debugging Bluetooth and Wi-Fi.

www.clarinox.com

Need a (robotic) hand?

Reduce the burden of deploying a 3D robotic bin-picking system

Manufacturers and systems integrators face numerous challenges when it comes to deploying robotic bin-picking systems. Robotically picking objects from cluttered bins or shelves for packaging, assembly, machine tending, and other complex manipulation tasks has proven difficult for nonexperts to deploy. However, advancements in 3D imaging technology and artificial intelligence (AI) software have now made it possible for technicians to implement bin-picking systems on their own factory floors.

When a company properly designs and implements a 3D-vision-guided robot, it can significantly enhance its operations. Moreover, the burden of deploying a bin-picking system has been greatly reduced thanks to advancements in underlying technologies, from robot arms and 3D imaging systems to AI software that combines optimal math-based motion planning and geometry algorithms with intuition-based machine learning algorithms that are more humanlike.

3D machine vision

To differentiate and pick loose, randomly oriented objects, a vision-guided robot must complete various complex steps. These include capturing the objects with a 3D camera, analyzing the parts in software, and understanding their orientation. The robot needs to receive information about an object's position, gripping points, and optimal movement path to execute the pick. When objects are piled randomly, the software must determine which object to pick, even when parts are only partially visible.

Additionally, when parts or objects are tangled, the robot arm might have to perform complex rotations or put the part down and regrasp it in the correct orientation. CapSen Robotics solves these problems with proprietary AI software that combines classic CAD matching techniques with proprietary machine learning, 3D vision, and motion planning algorithms. The software utilizes 3D models of objects that can either be provided by the customer or scanned-in using CapSen Scanner.

CapSen's PiC AI software employs geometry-based vision algorithms and machine learning techniques to continuously improve object detection accuracy. By utilizing 3D models, the AI software can discern how to accomplish the manipulation task at hand, which often requires holding and positioning a part in very specific ways so the part can move onto the next step of the process—assembly, packaging, or something else.

30 parts per minute

CapSen's PiC software offers consistent and complete control of the robot, end effector, and 3D cameras within a robotic cell, significantly reducing the integration burden of deploying a bin-picking system. Additionally, its image processing and planning times of less than a second make it the fastest software available, enabling PiC-powered cells to pick-and-place up to 30 parts per minute.

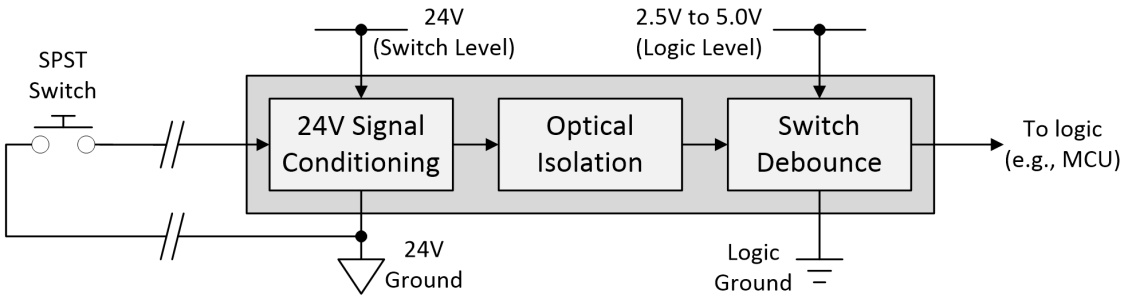
The hardware-agnostic AI software tackles the most challenging bin-picking problems by combining 3D vision with advanced motion planning and control software, providing robots with spatial intelligence without the need for custom programming for new parts. It also ensures collision avoidance and enables advanced motion planning tasks, such as detangling and assembly.

www.capsenrobotics.com

Jared Glover, CEO, CapSen Robotics

Who wants to debounce a 24V switch?

Current surge protection, voltage level translation, and debouncing—what's not to love?



Deep in the mists of time when I wore a younger man's clothes—circa the late 1970s—I was studying for my BSc degree in Control Engineering. This was a 4-year co-op course that commenced with nine months in college followed by six months in industry, and then do it all again. This was topped off by a final period of buffing and polishing at college, resulting in my emerging as a shiny new engineer.

My second stint in industry was at the research and development facility for a company called United Glass. Shortly before I arrived, someone had ordered a microcomputer based on the TMS9900 microprocessor from Texas Instruments (TI). The TMS9900 was one of the first commercially available, single-chip 16-bit microprocessors and it was awesome for its time. They told me to (a) learn how to use it and (b) think of things it could be used for. All I can say is that I was like a kid in a candy store.

After a couple of months at the R&D center, I was informed that I was being sent out into the field with my supervisor. We were to manage the installation of the new control systems in a glass factory that was in the process of being refurbished.

I don't regret much in my life, but I do regret not spending more time learning about the 24V switching used in that glass factory. This voltage level is used for switches in myriad industrial settings. The main idea behind using 24V is that these signals are less affected by electromagnetic noise and IR-drop than are their logic-level (5.0V or 3.3V) counterparts. This is particularly important when you consider that the switches may be mounted remotely with long wires connecting them to the control system.

Speaking of which, when a 24V signal from a switch meets the control system, it must be passed through voltage-level-converter, after which it needs to be debounced. "Debounced?" you cry, "but isn't that what you do?" Well, yes, as you so rightly observe, I am in fact the CTO for LogiSwitch. Switches bounce—that's what they do. We have a family of small ICs that remove bounce—that's what we do. Our chips come in 3-, 6-, and 9-channel flavors and in DIL or SMT packages.

The thing is that our ICs all work at logic-level voltages of 2.5 to 5.0V. Recently, I started thinking back to my student days in industry. In particular, I started to think that a small module, say around 0.75" by 1", that could accept a 24V signal from a switch and transform this signal into a debounced logic level equivalent would be a jolly useful thing to have.

What we are talking here is opto-isolation. Surge protection of up to 40A along with overvoltage and undervoltage protection on the switch side, augmented with noise rejection and debouncing on the logic level side.

The problem is that I'm not sure exactly what industrial users most desire. Do they want to support voltages other than 24V? Is a single channel module sufficient or would multi-channel modules also be of interest? To satisfy our curiosity we've created a short survey (https://rb.gy/95e31). We really would be most appreciative if you could take a few moments of your time to tell us what you think.

www.logiswitch.com

Balancing high power and high reliability analog design for aerospace applications

Apex Microtechnology has developed techniques and products to ensure high reliability in high power situations

Careful consideration of system reliability is essential when designing high-power analog components for aerospace and defense (A&D) applications. However, due to rigorous environmental conditions, device age, and modes of operation common in military systems, achieving both high power and high reliability can be a daunting task. Consequently, high power and high reliability often clash in A&D system designs.

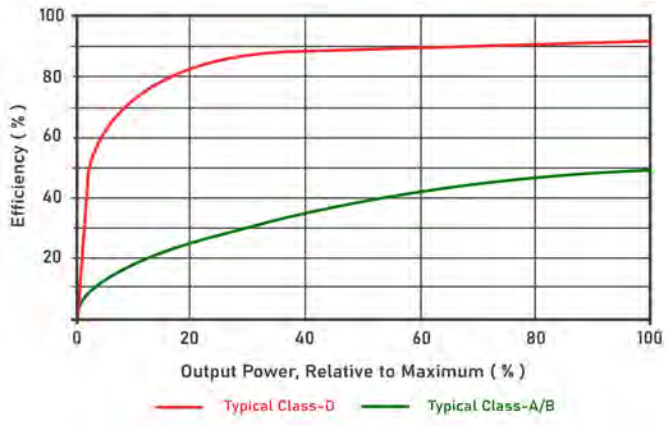
Simultaneously achieving high power and high reliability in analog design is extremely difficult for several reasons. The primary concern being the increased impact of device parasitics; that is, unwanted intrinsic electrical elements.

Metal-oxide-semiconductor field-effect transistors (MOSFETS)—which are essential components in analog electronics—exhibit parasitics due to their device structure. Parasitic capacitances and resistances in MOSFETs result in unwanted power consumption during device operation, thereby reducing the reliability of the analog circuits.

Integrated circuits also experience parasitics at higher levels, including those from device packaging, bond wires, substrate layouts, and printed circuit board (PCB) layouts. While these parasitics are usually negligible in low-power applications, they become significant in high-power A&D applications due to the higher voltages and currents involved. This can lead to increased losses, thermal generation, and device temperature, making it difficult to achieve high reliability at high power.

In aerospace and defense applications, specific architectural choices are necessary for high current and high voltage applications while still aiming for the highest possible reliability. For maximum efficiency in high power applications, design engineers often opt for class-D amplifiers. However, the tradeoff comes in the form of large amounts of electromagnetic interference from the surge currents (dI/dt) and peak voltages (dv/dt).

Large amounts of electromagnetic interference are unacceptable in A&D applications that require high sensitivity and accuracy, leading to the use of class-A/B amplifiers. While class-A/B amplifiers reduce electromagnetic interference, they come at the cost of efficiency, dropping from 90% range for class-D to approximately 50% range. Design engineers often need to compromise efficiency for the sake of minimizing electromagnetic interference and ensuring performance.



To combat these design challenges, Apex Microtechnology has developed several techniques and products to ensure high reliability in high power situations.

Silicon Carbide (SiC) MOSFETs

SiC—a wide bandgap semiconductor—offers reduced parasitics and a higher breakdown voltage than traditional silicon power FETs. SiC also offers superior thermal performance and reliability in high-power applications. Apex offers a product portfolio of integrated power modules, such as the SA111, SA310, and SA110 that incorporate Silicon Carbide technology to expand the boundaries of thermal efficiency and power density in analog design.

Packaging techniques

Apex ensures high reliability at high-power through rigid device packaging, utilizing base plates made from thermally conductive materials and pressure-sintered die attaches that ensures minimal voiding and thus greater thermal conductivity between substrate and base plates.

Through both techniques, Apex designs their amplifiers to sink heat away from the components, which lengthens device lifetimes and ensures proper operation, even in rigorous operating environments. In these ways and many more, Apex ensures its customers can balance the tradeoffs between high power and high reliability.

www.apexanalog.com

DC/DC converters for automotive applications

Voltage regulation subsystems are required throughout vehicles

Modern vehicles contain myriad subsystems that require local voltage regulation tailored to their specific application. These subsystems are found throughout the vehicle. They can range from high power active functions like headlights and climate control to low power passive modules such as keyless entry and tire pressure monitoring.

Each of these subsystems is designed to function under specific environmental limits within the greater automotive AEC-Q100 umbrella. Some are constrained by the available physical space, while others are designed with a focus on performance and efficiency. For DC/DC converters specifically, these unique requirements may include tolerance to wide swings in battery bus voltage, higher primary input voltages up to and including 60VDC, limitations on physical space available for supporting passives, and high conversion efficiencies under light loads and wide input/output ratios. To achieve these goals, ROHM has introduced two proprietary technologies into its DC/DC lineup specifically tailored to automotive needs: Nano Pulse Control and QuiCur.

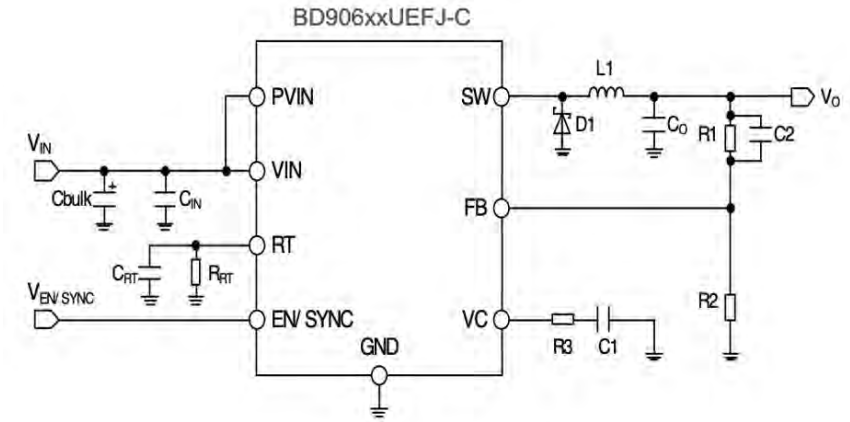
Nano Pulse Control technology

Nano Pulse Control is a DC/DC switching technology that offers the industry's smallest pulse width of only 9 nanoseconds. This is nearly 14X faster than a conventional converter.

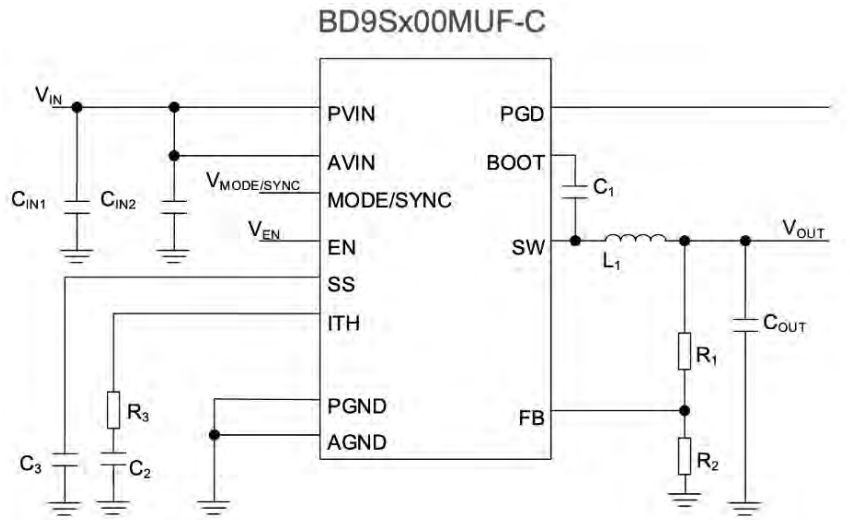
This miniscule pulse width allows ROHM's DC/DC converters to handle large input to output ratios, which makes them ideal for higher automotive bus voltages. Nano Pulse Control allows these converters to directly buck a 48V input rail down to a 1V output rail in a single stage. Competitor products, on the other hand, require an intermediate step utilizing two separate conversion integrated circuits (ICs). From a cost and space perspective, Nano Pulse Control is a clear industry leader that offers advantages in terms of efficiency and simplicity.

QuiCur technology

Integrated in ROHM's DC/DC and low dropout regulator (LDO) product lines, QuiCur technology is a circuit level technique that solves several of the main problems plaguing the feedback networks used to achieve high performance frequency response. This technology relies on introducing two dedicated error amplifiers into the feedback path. The second stage plays a particularly critical role by scaling its gain by the overall drive current.



Single stage regulating battery bus using the BD906xx series



Secondary supply regulation using the Nano Pulse Control BD9Sx00 series

The result is a much more flexible frequency response tradeoff, allowing the designer to choose between optimal stability, minimal undershoot, and reduced physical size.

For a given circuit design, using QuiCur immediately improves responses to rapid changes in load current. The voltage variability of the system is much lower when a sudden increase in load is encountered. This opens up the opportunity for a designer to use a smaller output capacitor without worrying about potential oscillation issues. The result is a high-performance regulator that is both smaller and more cost effective.

Primary DC/DC converter example

To illustrate the simplicity and rich feature set of ROHM's family of DC/DC converters, an example is shown for the BD906xx series, where the high voltage battery bus must be switched down to a much lower supply rail for an automotive infotainment system. This circuit can accept anywhere from 3.5V to 36V on the input side and—in a single stage—provide a regulated output down to 0.8V.

This regulator can supply up to 4.0A of current through the integrated output switch with an adjustable switching frequency between 50-600kHz. Available in a compact HTSOP package measuring just 4.9mm × 6.0mm × 1.0mm, the series is fully AEC-Q100 qualified and requires only a handful of supporting passive components.

Secondary DC/DC converter example

As is often the case, secondary supply rails must also be regulated down to lower voltages. In conventional technologies, two separate converters are usually chained in series to achieve the desired current rating while maintaining efficiency during light load operation. ROHM's Nano Pulse Control technology can accomplish this in a single stage with very few supporting components.

For example, using a BD9Sx00 series DC/DC converter to step a 5V rail down to a 0.8V core supply for an engine control unit (ECU). This device can provide up to 4.0A of current with integrated switches operating at 2.2MHz. The BD9Sx00 also features a "power good" signal and adjustable soft functionality that can be paired with a selectable light load mode. Available in a compact VQFN package of only 3.0mm × 3.0mm × 1.0mm, these DC/DC converters provide best-in-class performance for a wide range of secondary supply regulation demands.

Conclusions

Automotive electronic requirements present a unique set of environmental constraints that apply to a wide variety of voltage regulation solutions. Foremost among these are high input voltage combined with volumetric efficiency.

ROHM's proprietary Nano Pulse Control and QuiCur technologies enable DC/DC converters to thrive under these environments. They provide large input to output ratios, high performance frequency response, and an overall reduction in physical volume and supporting componentry. What's more, AEC-Q100 qualification makes these devices perfectly suited to the design requirements of many vehicle subsystems.

www.rohm.com

Unlock and monetize the potential of microcontroller data

Many applications need to process and refine their data at the edge

Data management at the edge cannot be overlooked because this will be instrumental in driving efficiency and providing real-time system insight through analytics, thereby helping embedded systems to make smart decisions.

Ignoring the need to modernize and manage data where it originates, on microcontrollers (MCUs) at the edge, will be a huge mistake. According to various reports, the exponentially increasing number of connected devices will create a data tsunami, and smart embedded systems must act as wave breakers for the ocean of data.

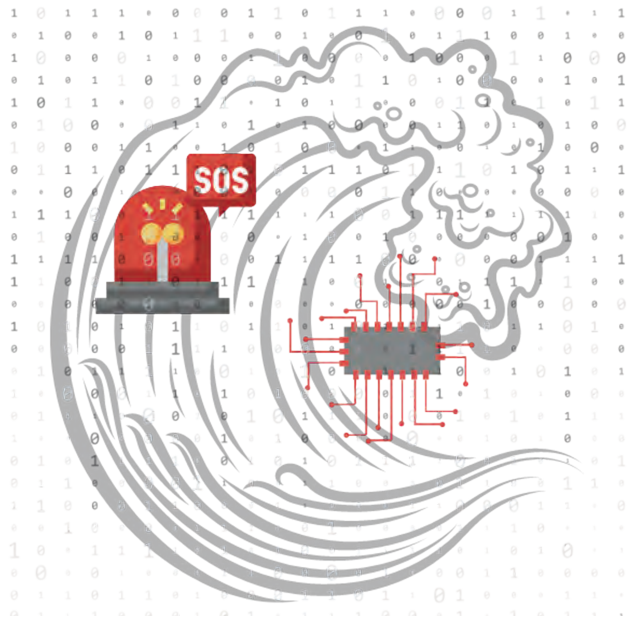
As part of this, MCUs will need flexible data management software that enables sensor data to be dynamically processed, stored, and communicated. This will enable each MCU to take on new responsibilities as part of the connected ecosystem.

When you build an application with MCUs, important considerations include memory footprint, total cost of ownership (TCO), and component integration. Generally, each MCU project uses a unique combination of hardware components that greatly influences software requirements. A major challenge for MCU applications is to process and refine the data at the edge with limited resources, so only relevant useful information is collected, organized, and stored. An effective solution will minimize footprint, data processing overhead, and long-term data maintenance costs.

Software components are typically deployed to an MCU as a unified firmware image. By design, the firmware is too infrequently updated to keep up with changes to the way sensor data should be analyzed and processed. Embedding a modern MCU database into the firmware provides the framework to organize data, run dynamically created data collection campaigns, and control device peripherals.

Unlocking the full potential of time series data pouring in from sensors into MCUs at the edge will require the right database. For a long time, applications built with MCUs performed in an isolated environment. However, with the arrival of the connected world and the internet of things (IoT) revolution, this has changed.

Connected MCU Devices Create a Data Tsunami



Sasan Montaseri, Founder and President, ITTIA

Building and embedding a database into firmware is not a simple operation. Great data management expertise and know-how is required to develop, test, and debug a data storage solution. The arrival of machine learning and artificial intelligence for MCU applications will also shift expectations. Preparing and performing all these tasks is not trivial and carries a significant cost.

Over the years, we have worked with many customers building applications with MCUs. Some customers require data storage for only simple data types; some are building complex edge systems for which data processing, security, and integration with other components play a vital role; and others want to accomplish much data

management and storage at the edge, but also to send data to the cloud.

We have seen manufacturers building various applications that collect log data and update configuration data to perform preventive maintenance, anomaly detection, and more. These embedded systems gain intelligence, make sense of data, and provide real-time insight. We've designed and developed our database for the IoT—ITTIA DB IoT—for MCUs organically, according to what we have learned.

Our main objective has always been modernizing data management for collecting, smoothing, and organizing real-time data at the edge. Our data management offers the filtering, aggregating, and smoothing of useful information, while also extracting relevant data from sensors and IoT nodes living at the very edge of the internet.

When you decide to consider a database for your application, it is important to make sure that you select a robust and verified database solution that has been designed from the ground up for tomorrow. Why? Because as you grow your business and develop additional requirements for integration and data exchange, obsolete solutions will only work with a portion of your data, not all of it. Data is a new currency. No one likes to go to the bank and have access to only a percentage of their funds.

Another important factor is security. There are many MCU application developers that purposely ignore adding security features to their products. Why? Because security adds memory footprint and they are unwilling or unable to allocate extra memory.

An additional essential issue is the type of data for which your application needs support. For us, time series data are the main citizens, so this is how we architected ITTIA DB. A time series database is a software system that is optimized for storing and serving time series through associated pairs of time(s) and value(s). The time series database is purpose-built to handle metrics, events, configuration, and logs.

When working on building platforms to manage MCU data, developers frequently ignore the importance of data management. Most systems built with MCUs will be deployed for a long time and—as the embedded systems grow—their data management complexities rise. It is important to select the right database vendor familiar with related challenges with the right database software for MCUs. The experienced database software vendor provides involvement and know-how for microcontrollers and offers a comprehensive review of data processing and management.

Processing and storing data closer to where it's generated and eliminating the need to send it all over the embedded system or to a centralized network offers great bandwidth and data maintenance cost savings. It also offers increased performance as data can be processed instantly.

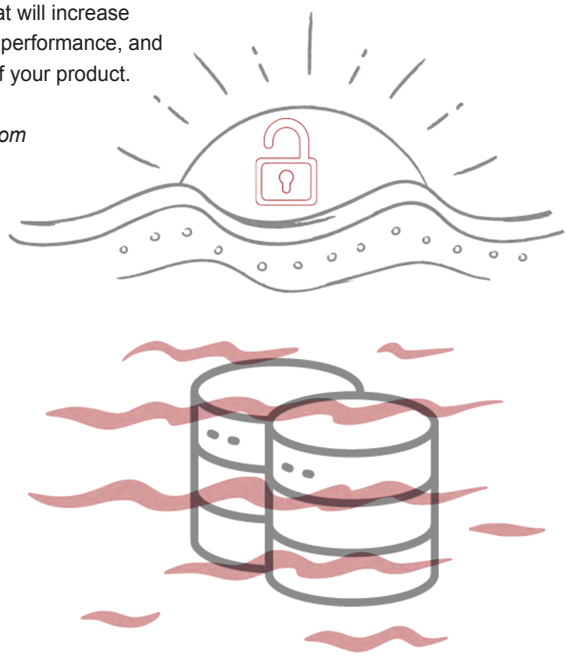
OEMs demand edge data management software that allows them to process and analyze data at the device so their system can gain insight and take immediate action. Even analytics and device training can be implemented on the MCUs.

Performing data management at the MCU edge allows these OEMs to have a great number of IoT devices working together, improving data management performance, and offering customers great cost savings.

You are building an embedded system that should last for ten, fifteen, or even twenty years (or more). We always encourage our customers not to underestimate the knowledge, cost, and complexity of the integration of MCU applications with databases. We believe one of your first tasks should be to determine the complexity of your data management and then select an appropriate database solution that will increase the power, performance, and longevity of your product.

www.ittia.com

"Unlocking the full potential of time series data pouring in from sensors into MCUs at the edge requires the right database"



Unlock the Full Potential of Time Series Data

Polymer capacitors—a superior alternative to MLCCs in every regard

The range of available polymer capacitors is both manifold and comprehensive

It is not only since the widespread introduction of 5G that the demand for multilayer ceramic chip capacitors (MLCCs) has been growing. In addition to significantly intensifying MLCC market growth, applications in the field of consumer electronics, data processing, telecommunications, and many others have even led to an industry-wide shortage in recent years.

All these factors contributed to more and more OEMs starting to look for ways to replace MLCCs with alternative capacitor types. This was exacerbated by the anticipation of an increasing demand due to 5G.

Some appropriate MLCC alternatives can be found within Panasonic's extensive industrial portfolio. As a leading manufacturer of polymer capacitors with a long design-in expertise, Panasonic's SP-Caps and OS-CONs are as well worth a closer look, as are POS-CAP tantalum polymer capacitors, along with the manufacturer's polymer hybrid aluminum electrolytic capacitor technologies.

For conductive polymer capacitors, the fields of application have broadened remarkably in recent times. Polymer capacitors (as well as conventional aluminum electrolytic capacitors) stand out with large capacitance figures and excellent bias characteristics that are clearly outperforming their multilayer ceramic chip capacitor counterparts.

MLCCs are surface-mounted, fixed-value capacitors with alternating layers of metal and ceramic serving as dielectric. MLCCs are used in a higher volume than any other type of capacitor, in everything from smartphones to electric vehicles.

Panasonic's industrial polymer capacitors have already been proven as a highly relevant alternative for customers seeking to save printed circuit board (PCB) cost and real estate. These polymer-based devices offer a performance edge over conventional electrolytic and ceramic capacitors when it comes to the following:

- Electrical characteristics
- Stability
- Longevity
- Reliability
- Safety
- Life cycle cost

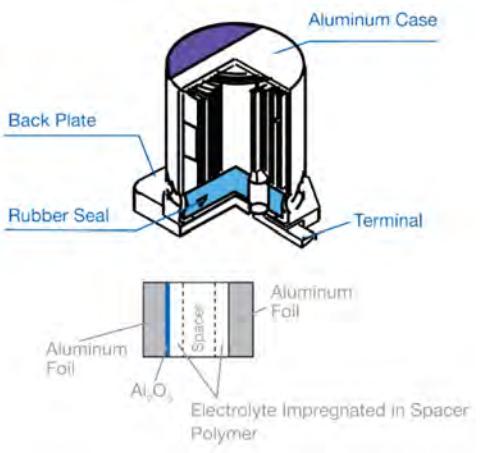
The various types of polymer and hybrid capacitors have very specific advantages and benefits in terms of their ideal voltages, frequency characteristics, operational conditions, and other application requirements.

If we include hybrid devices, there are basically four main varieties of polymer capacitors, each composed of different electrolytic and electrode materials and each offering different packaging and application targets. A brief overview is as follows…

SP-Caps: The new flagship of ultra-low ESR

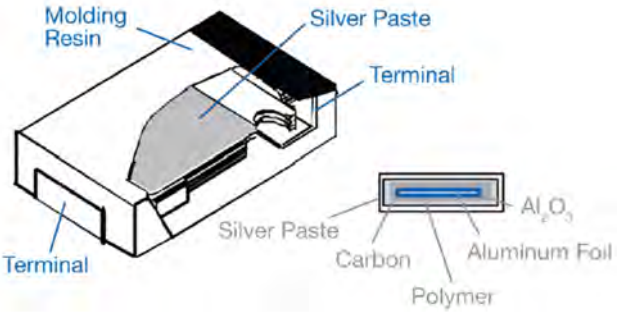
Using a conductive polymer as the electrolyte and an aluminum cathode, the distinguishing electrical characteristic of these polymer capacitors is their extremely low equivalent series resistance (down to 3mΩ), which is among the lowest in the industry.

SP-Caps cover a voltage range from 2 to 6.3V and offer capacitances between 2.2 to 820µF. Packaged in molded resin as a compact surface-mount device (SMD), these layered polymer capacitors come in a low profile. As a result of their electrical and form factor characteristics, they suit a variety of handheld electronic devices or other applications that require a low-profile capacitor that will not interfere with a nearby heat sink.

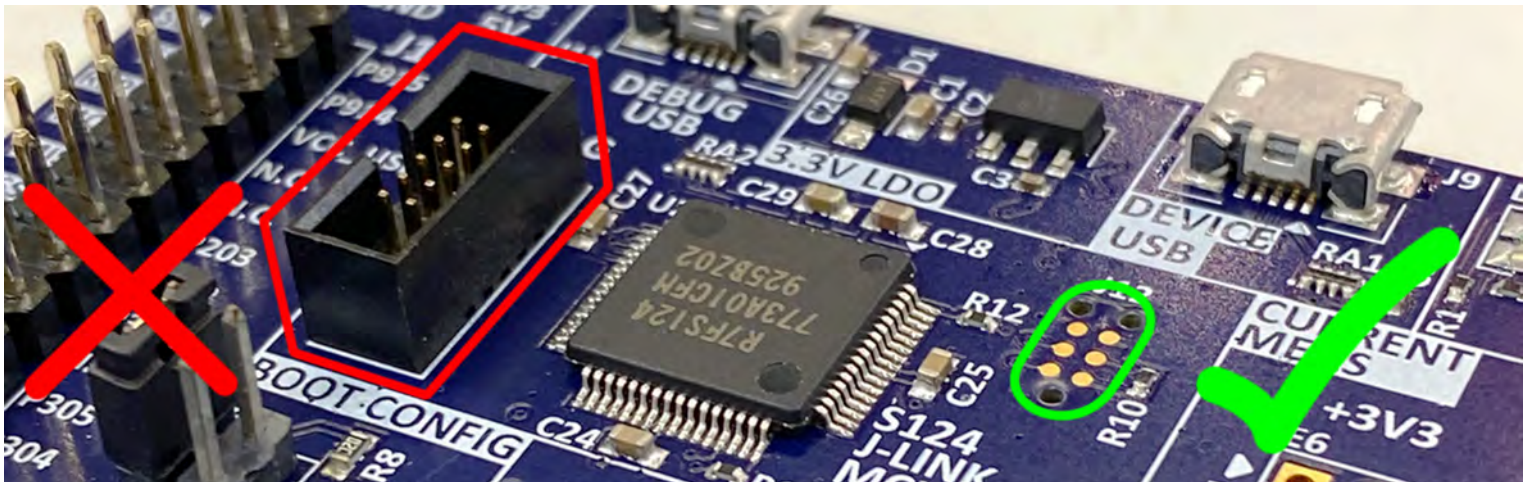


OS-CONs: Large capacitances and long lifetimes

Like SP-Caps, OS-CON capacitors are also based

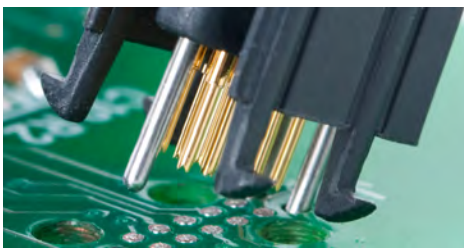


Tag-Connect



No Header! No Brainer!

JTAG Connector Plugs Directly into PCB!!



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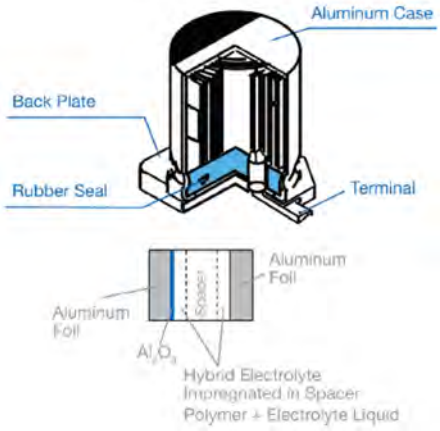
STLink-V3 for illustration only

on conductive polymers and aluminum, but they have a wound foil structure. These wound polymer capacitors cover a wider range of voltages and capacitance values than other types of polymer capacitors. Voltages extend from 2.5 to 100V, while capacitances run from 3.3 to 2,700µF.

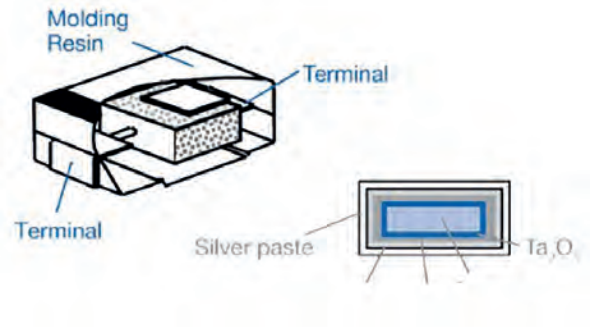
In addition, their long lifespan is one of the factors that causes them to be preferred for use in servers and base stations. For example, with lifetimes of 20,000 hours at 105°C, the SVPT series offers a unique solution for such applications.



Hybrid capacitors: The best of both worlds

Hybrid capacitors consist of a combination of a liquid and conductive polymer to serve as the electrolyte and aluminum as the cathode. The polymer offers high conductivity and a correspondingly low ESR. The liquid portion of the electrolyte, meanwhile, can withstand high voltages and provide higher capacitance ratings due to its large effective surface area.

These hybrid capacitors offer a voltage range from 25 to 80V and capacitances between 10 and 560µF. At 11 to 120mΩ, ESR values for hybrids are higher than other types of polymer capacitors, but still very low considering the higher power applications they address.



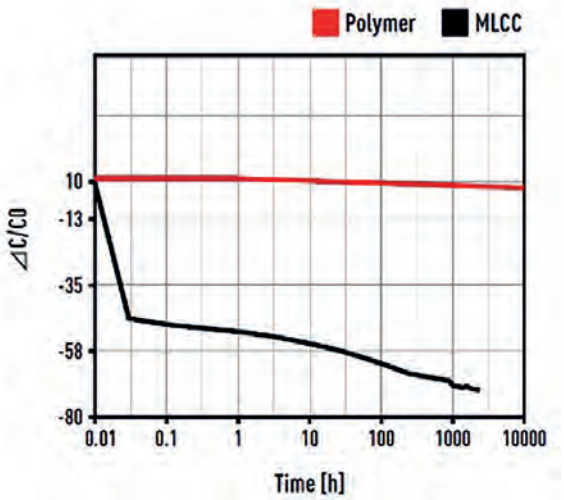
POSCAPs: The capacitors of choice for compact devices

These types employ a conductive polymer as the electrolyte and have a tantalum cathode. They span voltages from 2 to 35V and capacitances from 3.9 to 1,500µF. They also impress with a low ESR, with some of our POSCAP capacitors exhibiting ESR values as low as 5mΩ.

Packaged in a molded resin case, these tantalum polymer capacitors are among the most compact options available on the market. Having said this, although they are indeed compact, a wide range of sizes is available for this capacitor type.

Advantages of polymer capacitors

Let's take a closer look at polymer capacitors to see what makes them outperform MLCCs and other technologies.



Capacitance density and stability vs. DC bias: The MLCC exhibits strong capacitance dependence on DC bias due to the ferroelectric dielectric materials used for MLCCs.

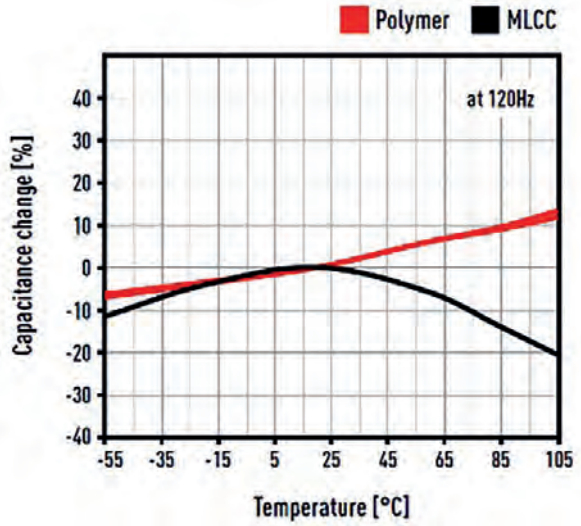
By comparison, polymer capacitors have no such problem and remain stable over time. This specific advantage allows a significantly lower part count when using polymer capacitors instead of MLCCs, thereby saving precious PCB space, reducing steps during the production process, and lowering costs.

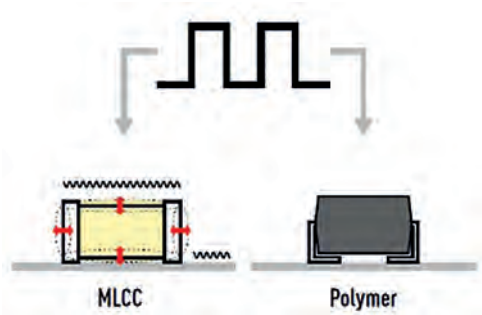
Stability vs. temperature: Typical temperature characteristics for MLCCs involve the curve changing in various ways within the tolerance range of each product. By comparison, in the case of polymer capacitors, the capacitance grows in a linear fashion in response to the increase of temperature.

The temperature characteristics of MLCCs differ according to the dielectric type, but all of them suffer aging failure by exhibiting temperature dependency and require lower operating temperature.

Ceramic capacitors are brittle and sensitive to thermal shock, so precautions need to be taken to avoid cracking during mounting, especially for high-capacitance large MLCCs. Typically, ceramic capacitors support a temperature range from –40°C to 85°C, while their capacitance varies about from +5% to –40%, being in the optimal range around a low temperature of 5 to 25°C.

Also, polymer capacitors have great development potential to achieve higher ratings in terms of density, field stress, and temperature (which is currently limited to 125°C) due to their working mechanism





and dielectric materials advancement. Higher dielectric constant polymers enable a high energy density.

Piezoelectric effects: A MLCC deforms (contracts or expands) when exposed to voltage. This MLCC characteristic is called the "inverse piezoelectric effect" (the reverse of a piezoelectric effect).

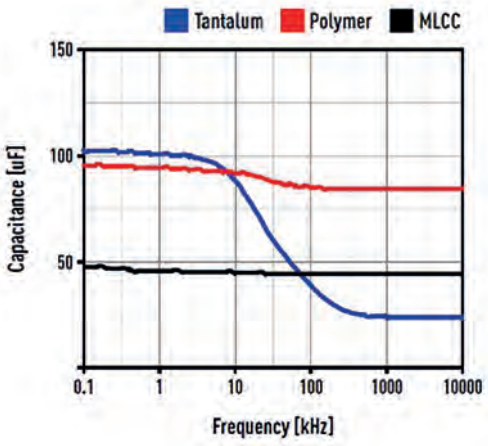
The DC voltage output from an AC adaptor or switching power supply causes a ripple voltage in some cases. In the case of a MLCC capacitor, if the frequency of the ripple voltage is within the audible frequency range, the inverse piezoelectric effect may result in the emission of a screeching noise.

By comparison, a conductive polymer capacitor has no inverse piezoelectric effect and therefore does not cause any noise emissions or micro-vibrations.

Stability vs. frequency: Different technologies exhibit different change in capacitance profiles over a wide frequency range.

Unlike tantalum capacitors, polymer capacitors exhibit very similar frequency response performance to their MLCC counterparts.

Robustness: Cracks in ceramic surface-mount technology (SMT) components limits assembly reliability and yields. These cracks manifest themselves as electrical defects in the form of intermittent contacts, variable resistance, loss of capacitance, and excessive leakage currents. This is why MLCCs are exposed to different reliability tests including thermal shock, board flex (bending), and biased humidity tests, etc., depending on the targeted applications.



Among the various reliability tests, the board flex test evaluates the mechanical resistance to cracking when MLCCs are subjected to bending stress on the PCB onto which the MLCC is soldered. Such bending of the PCB can occur frequently during (and between) manufacturing steps and during operation under temperature variations.

Ceramics are strong in compression but weak in tension. Thus, when a soldered MLCC experiences excessive board flex, a crack is easily generated in the element. A flex crack can cause an electrical conduction between opposing internal electrodes. It is also possible that a fail-open can progress to a fail-short with continued product usage over time. If a crack on a capacitor element progresses to a short circuit failure, it may cause problems such as heat generation, smoking, or ignition. This means it is imperative to take counter measures against flex-induced faults, particularly in equipment where reliability is essential.

Safety: Most ceramic capacitors have a fairly high voltage rating. If the capacitor experiences a voltage between its terminals higher than its rated voltage, the dielectric may break down and electrons will flow between the thin metal layers inside the capacitor, creating a short.

Fortunately, most ceramic capacitors are built with a hefty safety margin and do not experience any sort of catastrophic failure (such as exploding). However, the generally accepted "rule-of-thumb" dictates that you should derate ceramic capacitors by 50%. This means that if you are expecting to have a maximum of 5V between the capacitor's leads, then you should use a capacitor rated for 10V or more.

By comparison, no derating needs to be considered for polymer capacitors. Furthermore, these devices can usually withstand a 15 to 25% surge voltage.

Conclusion

The range of polymer capacitors that can be used as MLCC alternatives is manifold and comprehensive. There are specific types for specific requirements. What they all have in common, however, is that they are a contemporary choice in terms of electrical performance, reliability, durability, and safety, not least when looking at their overall lifetime cost.

To put things even more simply, polymer capacitors are not only a good alternative in case of supply shortages of other products, but are actually the first choice for the design process of many modern applications.

na.industrial.panasonic.com

"Polymer caps are not only a good alternative in case of supply shortages of other products, but are actually the first choice for the design process of many modern applications"

The need for ultra-long-life batteries

Ultra-long-life batteries can power IIoT-connected devices up to 40 years

At the core of the industrial internet of things (IIoT) are remote wireless devices being deployed at remote sites and in extreme environments. In these situations, extended battery life is essential to achieving an acceptable return on investment (ROI). These applications include AMR/AMI metering to M2M, SCADA, tank-level monitoring, asset tracking, environmental sensors, and more.

Extended battery life is critical wherever battery replacement is prohibitively expensive or impossible. To accomplish this, design engineers must employ a variety of techniques: with the device predominantly operating in a "standby" state that draws nominal current, utilizing some type of low-power communications protocol (e.g., WirelessHART, ZigBee, LoRA) coupled with low-power chip sets and proprietary techniques to minimize energy consumption during "active" mode and—most importantly—specifying a battery with a very low annual self-discharge rate.

The vast majority of low-power devices draw average current measurable in micro-amps with periodic pulses in the multi-amp range. These devices are predominantly powered by bobbin-type lithium thionyl chloride ($LiSOCl_2$) chemistry, which offers unique performance characteristics, including extremely high capacity and energy density (supporting product miniaturization); an extended temperature range of –80 to +125°C (ideal for harsh environments), and an extremely low annual self-discharge rate (enabling up to 40-year battery life).

Exceptionally low self-discharge is achieved by harnessing the passivation effect, which occurs when a thin film of LiCl surrounds the anode to reduce the chemical reactions that cause self-discharge. Each time the battery starts to draw continuous current the passivation layer begins to dissipate, which is a continually recurring process.

The method by which a battery is constructed affects its ability to harness the passivation effect. For example, a superior quality bobbin-type $LiSOCl_2$ cell can retain roughly 70% of its original capacity after 40 years. By contrast, a lower quality cell has a self-discharge rate of up to 3% per year, losing 30% of its nominal capacity every 10 years, making 40-year battery life unachievable. Extended battery life is necessary wherever battery failure is highly problematic. A prime example is AMR/AMI utility metering, where large-scale battery failures can compromise billing systems, disable remote shut-off capabilities, and overwhelm field service crews.

Two-way wireless communications demand high pulses

Increasingly, IIoT-connected devices require periodic high pulses to power two-way wireless communications. Standard bobbin-type $LiSOCl_2$ batteries serve as the ideal foundation by delivering exceptionally low self-discharge. However, these standard cells cannot generate the required high pulses due to their low rate design. This challenge can be easily addressed with the addition of a patented hybrid layer capacitor (HLC). This hybrid approach uses the standard $LiSOCl_2$ cell to deliver low-level background current while the HLC generates the high pulses required to power wireless data communications. The patented HLC also features a unique end-of-life voltage plateau that can be used to generate low-battery status alerts that permit more pro-active maintenance.

High self-discharge can take years to become apparent, so thorough due diligence is required when comparing batteries. Start by demanding long-term test results, in-field data involving comparable devices with equivalent energy needs and environmental conditions, and multiple customer references.

Paying a little extra for an ultra-long-life lithium battery generally pays off in the long run by increasing your lifetime ROI while improving product reliability and data integrity.

www.tadiranbat.com

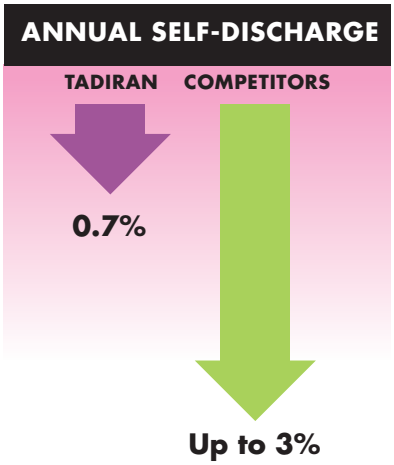
"Extended battery life is critical wherever battery replacement is prohibitively expensive or impossible"

IIoT devices run longer on Tadiran batteries.

PROVEN
40
YEAR
OPERATING
LIFE*

Remote wireless devices connected to the Industrial Internet of Things (IIoT) run on Tadiran bobbin-type $LiSOCl_2$ batteries.

Our batteries offer a winning combination: a patented hybrid layer capacitor (HLC) that delivers the high pulses required for two-way wireless communications; the widest temperature range of all; and the lowest self-discharge rate (0.7% per year), enabling our cells to last up to 4 times longer than the competition.



Looking to have your remote wireless device complete a 40-year marathon? Then team up with Tadiran batteries that last a lifetime.

TADIRAN BATTERIES

* Tadiran $LiSOCL_2$ batteries feature the lowest annual self-discharge rate of any competitive battery, less than 1% per year, enabling these batteries to operate over 40 years depending on device operating usage. However, this is not an expressed or implied warranty, as each application differs in terms of annual energy consumption and/or operating environment.

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Preventing extinction through remote AI

How Conservation X Labs solves its most significant challenges

To say that artificial intelligence (AI) and machine learning (ML) have changed the world would be putting it lightly. Not since the early days of smartphones has technology garnered such widespread innovation and disruption. Yet, for all the good AI and ML have done, these technologies have also generated their fair share of unrest, the root of which is the fear that AI may one day entirely supplant human intelligence.

Fortunately, this fear is largely unfounded. While AI and ML will inevitably replace some careers, the reality is that machine intelligence is at its best when augmented by human intelligence. The two are—and always will be—complementary, with each capable of performing tasks that the other cannot.

This is particularly evident where monitoring and data management are concerned. AI is capable of analyzing and organizing an immense volume of data in real time and at a speed well beyond the capacity of any human. The potential applications of this functionality are unprecedented… provided one can overcome the challenges.

"One [compelling use case for ML] is wildlife conservation," writes Sam Kelly, Conservation Technology Director & Project Lead: Sentinel AI at Conservation X Labs. "Organizations that work in the wildlife conservation space are performing ML inference on the edge to study, track, and protect endangered species. Tools such as tracking cameras and environmental sensors are producing data that can be coupled with ML to better inform conservation and protection efforts."

Founded in 2015, Conservation X Labs is a technology startup that leverages edge AI to help prevent the sixth mass extinction. Although wildlife conservationists have worked tirelessly to protect the environment, their efforts have not been enough. They simply haven't been able to operate on the scale or at the pace necessary to prevent large-scale habitat and wildlife destruction.

Nicholas Greene for Mouser Electronics

"To address the looming threat of a sixth mass extinction event, Conservation X Labs opted to develop a new line of intelligent sensors and cameras. This, however, was only half the battle—after all, it doesn't matter how intelligent a device is if it can't stay powered. "

Through collaboration with the ML development platform Edge Impulse (edgeimpulse.com), Conservation X Labs intends to change that.

Computation without the cloud

"[Conservation X Labs] focuses on the drivers of the [extinction] crisis, not the symptoms, to confront the issue at its source," Kelly continues. "To support these efforts, Conservation X Labs [has] engineered innovative monitoring and tracking technologies such as Sentinel."

Built with Google's Coral AI toolkit, Sentinel is designed to augment existing wildlife-tracking tools and systems such as trail cameras and audio recorders. It leverages satellite and cellular networks to provide conservationists with comprehensive, real-time data on everything from invasive species to disease to possible wildlife trafficking. Sentinel represents one of Conservation X Labs' two flagship products—the other being the Nucleic Acid Barcode Identification Tool (NABIT), which provides on-demand genetic diagnostics in the field.

Kelly notes that real-time monitoring and analysis represent the foundation of tools like Sentinel. This means that such devices must be capable of low-latency computation, which—in most cases—requires a connection to a cloud data center. This wasn't an option for Conservation X Labs.

"Wildlife detection and tracking devices are often deployed in isolated and remote locations," Kelly explains. "Out in the field, cellular connectivity is virtually nonexistent. For wildlife conservation devices to do their job most effectively, they need the longest battery life possible, as battery replacements for remotely deployed cameras are an unrealistic option."

Conservation X Labs identified edge computing as the most likely technology to support its needs; this would allow the company to limit the amount of data sent and received by its remote devices, thereby preserving battery life. It would also ensure that the systems could operate without requiring a constant network connection. Unfortunately, even as it addressed these challenges, it encountered several more:

- For each animal in a region, Conservation X Labs had to develop both a data set and a machine learning model.
- Machine learning is an industry in flux, with constantly evolving libraries, dependencies, and algorithms.
- Conservation X Labs lacked the necessary workforce to maintain and operate a platform such as Sentinel.

"After trying many other tools, Conservation X Labs discovered Edge Impulse," explains Kelly. "Edge Impulse's platform makes the development, optimization, and deployment of ML models at the edge extremely easy and accessible. The platform enables developers to manage the workload at a high level, encompassing everything from data preparation and data selection to model selection, model training, and model deployment, including device-specific binaries."

Enabling a smarter approach to wildlife conservation

We can no longer afford to ignore the impending extinction crisis. As with climate change, we are rapidly approaching the point of no return. If there is any hope of pulling our world back from the brink, conservationists must adopt a new approach, one supported and empowered by smart technology uncoupled from networks and data centers.

Yet this technology is not without its challenges, from battery life and connectivity to training and lifecycle management. Through edge computing, Conservation X Labs managed to overcome the former two roadblocks. As for the latter, it came down to selecting the right partner.

"Thanks to Edge Impulse, Conservation X Labs developed edge devices to monitor, detect, and ultimately protect endangered wildlife," Kelly concludes. "Conservation X Labs believes these advanced technologies can help restore balance to the natural world and prevent future crises from occurring."

www.mouser.com
www.conservationxlabs.com

A simple solution to high power density applications

New high-density power module technology for FPGAs, SoCs, and ASICs simplifies design

As semiconductor technology shrinks, it's becoming increasingly difficult to meet the power demands of integrated circuits (ICs) in less available space. Recent power solutions trade off power density against ease of use, but TDK has created new power modules without these compromises.

TDK's new µPOL power modules have power circuitry built into a substrate to create a module that can be mounted on either the front or the back of a printed circuit board. This approach realizes an easy-to-use solution delivering 15W in 49 mm^3 or 1 watt per cubic millimeter of power.

Ease and speed of design

To use these products, designers need only specify input capacity, output capacity, and—if not using a preset output voltage—a voltage divider, and then match requirements to an available µPOL solution.

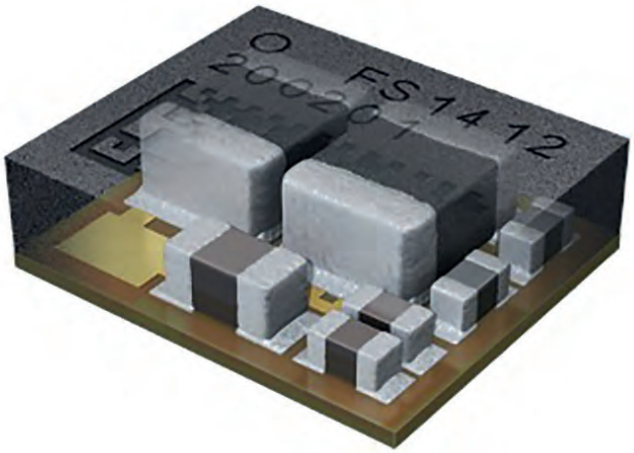
Micropower modules are available from 0.6V to 5V output voltage to meet the design requirements of most applications in communication infrastructure, data computing, IoT, embedded vision, real-time signal processing with FPGA, robotics, and AI. TDK provides layout files for the key FPGAs used in these applications.

The path to power density

These µPOL micropower modules are based on TDK's proprietary semiconductor embedded *sub*strate (SESUB) technology. Construction begins with an embedded IC, which includes a DC-DC regulator, MOSFETs, and a driver. A copper heat plate is added to the die, embedded for optimal thermal flow from the die to the package, providing 4X to 8X better thermal design than other technologies. This assembly is incorporated directly into a SESUB, four-layer, 300-micron thick substrate.

This approach eliminates the need for troublesome wire bonds and delivers the additional benefit of high reliability against shock and vibration, making the µPOL ideal for industrial and mobile applications like drones. The thermal sink positioned on the bottom of

Tony Ochoa, director of marketing, µPOL DC-DC product group, TDK



TDK's new µPOL power module

the SESUB allows heat to flow directly into the board for better thermal flow while minimizing the space required. This architecture allows the module to be operated at full-rated current without requiring forced airflow.

Designing with µPOL

TDK provides a power map that identifies the µPOL power module recommended for each voltage rail requirement. It also indicates where common modules can be used in multiple locations on the same design to help reduce costs. Maximum output voltages depend on output currents, and—in analog mode—voltage programming is not necessary; a simple resistor change is all that's required.

Design tools

TDK has created multiple design tools for designers to use. Information is available at www.us.tdk.com/POL, where users can find starter power schematics and PCB layout templates in Ultra Librarian along with links for:

- AMD Xilinx FPGAs
- Intel Altera FPGAs
- Microchip Devices
- Lattice FPGAs
- Efinix FPGAs

These designs address each of the key power rails, recommend the best module for each power rail, and provide a solution that has been tested by both TDK and the FPGA supplier.

In addition to FPGAs, power schematics for other communication processors and Ethernet chipsets are provided:

- Marvell Armada and Cavium Octeon Arm processors
- NXP LayerScape QoriQ Arm processors
- Broadcom Ethernet controller
- Intel Ethernet controller
- Marvell Ethernet PHY

Selecting components

Once the starter schematic has been chosen, the designer must determine the input and output capacitors. The capacitors provided in the baseline solutions address typical requirements. However, although they have margin built in, they still need to be thoroughly evaluated if V_{IN} is noisy or unstable and/or if V_{OUT} supplies a high transient load.

Designers must determine the actual capacitance value (bulk capacitance for energy storage), the type of capacitor technology to be used, and the allowable parasitic values of the capacitors in terms of equivalent series resistance (ESR) and equivalent series inductance (ESL). Additional output capacitors may be required if the design could experience large di/dt transient events. Resistor divider values should be verified for the final output voltage by point-of-load measurements.

Component design and layout

The distribution of capacitors at the output is also important to minimize circuit board parasitics, as these can impact the speed of supply of stored energy (current) to the electrical load when needed.

Connections to each power plane should be kept simple to ensure no ground loops occur and to avoid parasitic inductances and/or capacitances. It is also recommended that the input communication pins be electrically grounded on the PCB if I2C or PMBUS are not used in the application.

While TDK's µPOL power modules have current ratings that do not require additional airflow, designers still need to include sufficient PCB thermal vias, properly designed and located, to adequately support the system power while addressing thermal requirements. It is also important to consider copper weight on the PCB and the number of layers, since both impact the thermal performance.

µPOL construction

The 15W-rated modules all have common pinouts and pad layouts for ease of layout. They are available with pre-programmed standard output voltages that reflect the more common voltage rails or, in the case of the FS1406-0600 and FS1412-0600, as customer-configurable output voltage devices using resistors.

Summary

With best-in-class thermal performance and the highest power density for small spaces, TDK's µPOL power modules offer design and performance advantages while being easy to use and fast to implement.

www.us.tdk.com

"With best-in-class thermal performance and the highest power density for small spaces, TDK's µPOL power modules offer design and performance advantages while being easy to use and fast to implement"

The need for versatile multicore chip technology

Flexible multicore chips present significant opportunities for innovation

The semiconductor industry faced a gauntlet of challenges in the past year, ranging from millions of unbuilt cars to multitudes of delayed iPhones. The increased scarcity of electronics across several markets hasn't escaped the notice of everyday consumers. In fact, it's provided a wake-up call for many consumers who may not have been aware previously just how dependent on chip technology are a huge range of the products they use.

However, inefficiencies in supply chains have obscured another major problem in the semiconductor market—chip programmability. While several global powers are currently committing huge resources to addressing the fundamental supply and demand of silicon hardware, the complexity of programming multicore chip architectures remains unsolved.

Devices are getting smarter and more interconnected, presenting new market opportunities with distinct requirements. This means rigid architectures with differing programming environments won't be sufficient to keep pace with evolving demands for innovation. Moreover, manufacturers are under increasing pressure to balance the required time, cost, and reward of developing new products. This issue of chip programmability poses as much of a challenge to the semiconductor industry as does the physical supply chain issues that have dominated headlines. Left unaddressed, the programmability challenge will become a major break on further innovation.

But with such a multifaceted challenge—encompassing a huge variety of multicore architectures—where does the industry need to focus its attention?

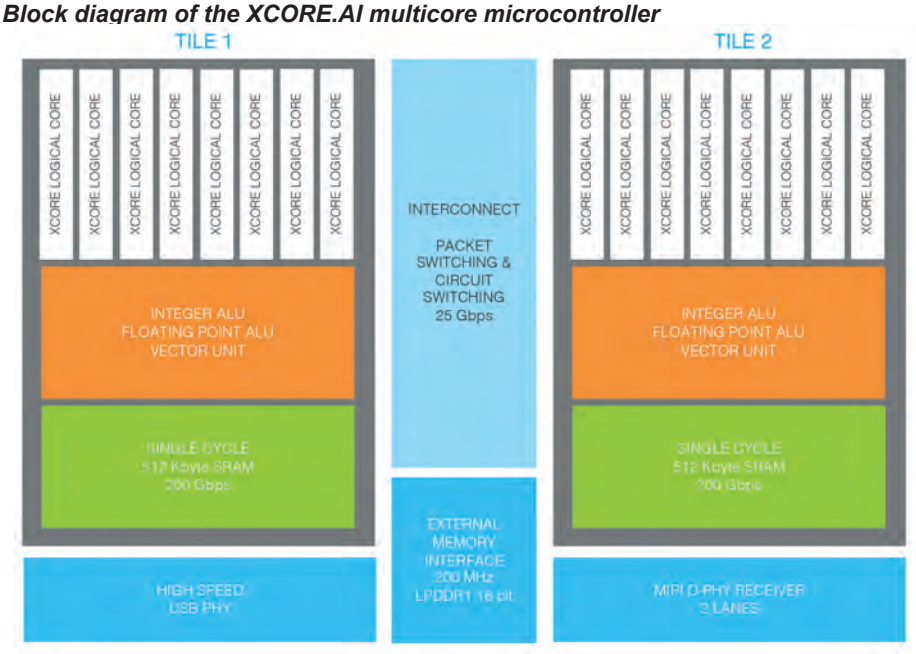
#1: Increased time to market and burgeoning costs—fragmented markets: The most apparent design challenge is the intricacy of today's SoCs, which integrate entire electronic systems. Software operating on heterogeneous multicore processors is complex and necessitates custom programming, validation, and verification. This slows the design process, increases the time to market, and—ultimately—places a greater financial burden on manufacturers.

Aneet Chopra, VP of Product, XMOS

With the industry increasingly having to cater to the specific needs of an ever-growing range of applications, the notion of a "one size fits all" approach to programming becomes unfeasible. This means it's impossible to assure product designers they'll have a familiar environment to work with. Moreover, it becomes cost impractical to serve each unique market with a dedicated processor, especially in a fragmented intelligent IoT market.

#2: Rigid architectures complicating design: Moreover, there's no guarantee that the end-product will be futureproof once the programming process is complete. Devices are evolving and becoming more intelligent, which entails even more precise and unique

Block diagram of the XCORE.AI multicore microcontroller



specifications, and yet system structures are expected to become more and more adaptable. At present, it's not uncommon to embark on custom development which takes some months, only to find it isn't compatible with the most recent iteration of SoC architecture.

With the design of physical devices presenting many variables, and the need to optimise how the processor performs, even minor adjustments can necessitate a re-design from scratch.

#3: The myth of reusability of some processors: Despite these design difficulties, there's an enduring myth that keeping within a specific group of processors will deliver re-usability, while switching between processor families is overly complicated due to diverging sets of instructions.

Some may raise the alleged commonality of Arm-based processors to provide the flexibility of a truly interchangeable system, but that would be a mistake.

As a result of each SoC being unique, there's no truly homogenous programming model across different platforms that's consistently available to engineers. IoT architectures and bespoke processors present different requirements and challenges, necessitating different toolsets and techniques to be used for different purposes, even if they use a common Arm core, for example.

A common framework within which architectures can be interchanged is far too rare. This is due to the difficulty of attributing a programme to multicores while balancing across them, with the interfaces typically used to do so being complex and inaccessible.

So, in summary, complicated SoCs operating on multicore processors take years to release, are often impossible to modify once they're available, and lack the accessibility and adaptability to even facilitate amends. All of this presents an impossible challenge for manufacturers aspiring to shape their product as envisioned.

The creative process

Addressing these challenges means seeing the bigger picture. It isn't feasible to invest time or significant sums of money in long term projects aiming at perpetually moving targets. We need a more agile and accessible development model.

Ultimately, this means realising a new design environment that can provide a genuinely common frame of reference between different products. This framework will need to ensure that it's possible to configure different types of processing simultaneously, whether for general purpose, digital signal processing (DSP), artificial intelligence (AI), or low-latency real-time deterministic input/output (I/O). This needs to be made possible via the same tools and languages, and with robust and reliable execution characteristics.

Given the complexity and specific requirements of new markets, real-time operating systems like FreeRTOS in combination with traditional embedded programming practices meet most of these requirements. These systems provide the level of familiarity and flexibility expected by engineers, while making it as easy to understand as possible. However, we still need to consider the proper means to apply this system within multicore architectures.

To make good on its versatility and accessibility, this environment needs to rest upon more flexible hardware platforms that facilitate the use of different processing types, regardless of the engineer's requirements.

Programming multicores won't be as challenging provided we can develop readily available architectures that are based on the needs of engineers, but without the caveat of continually learning new languages, architectures, or tools.

New hardware, new possibilities

The technical and supply-related challenges facing the chip industry have highlighted the need for versatile, cost-effective chip technology that can keep pace with evolving market demands for innovation. While the industry is currently focused on addressing supply and demand issues, the complexity of programming multicore chip architectures won't go away.

The possibilities afforded by flexible multicore chip technology present significant opportunities for innovation in various industries. By addressing programming challenges and investing in a more flexible development model, manufacturers can unlock the full potential of this technology and drive the industry forward, while giving rise to new use cases in smart homes, offices, and cities.

The XCORE.AI offers the features and benefits of multicore microcontrollers, application processors, AI accelerators, and FPGAs

Within smart homes, multicore chips can optimise local devices and allow for intelligent automation, allowing for energy-efficient heating systems and general convenience to occupants. In the office, multicore chips can enable voice conferencing and other communication technologies that are essential in today's remote work environment. Meanwhile, in smart cities, multicore chips can facilitate intelligent traffic management and other critical infrastructure to ensure our safety.

Whether applied in the developing smart home market or within established niches like voice processing, semiconductor device design and manufacturing would benefit significantly from a versatile platform that is easy for engineers to use.

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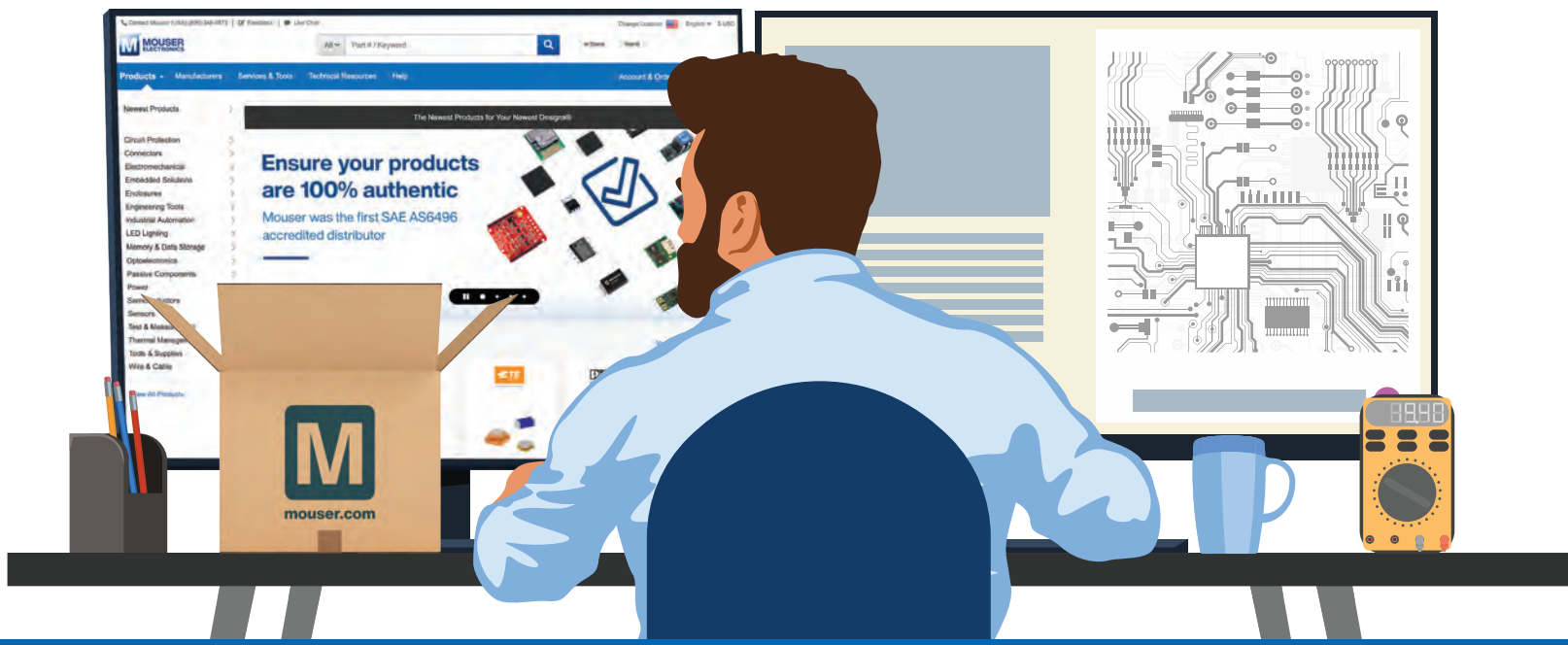

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