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JANUARY 2024

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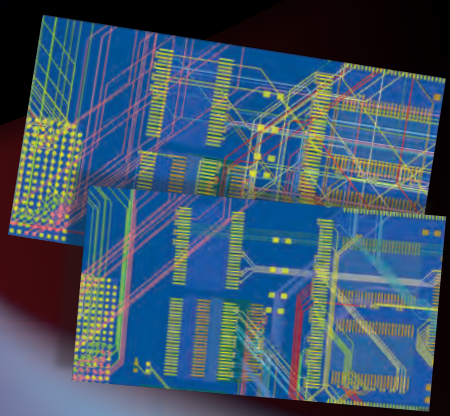

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EDITORS WORD

Happy 2024!

Every time we greet a new year, I find myself thinking how much things have changed technology-wise since the 1960s when I was a little lad growing up in Sheffield, England.

Take telephones, for example. As Christmas grew closer, my aunt, who lived round the corner, would come to our house, then she and my mom would attempt to call one of the aunts in Canada. This involved calling the local operator in Sheffield, who would transfer them to the international operator in London, who would connect to the international operator in Canada, who would transfer to the local operator in Edmonton, Alberta, who would attempt to call the aunt in question.

If the aunt was out, it was "game over" (voicemail didn't arrive until the late 1970s). Even if the aunt was in, this wasn't "The Call." This was just to arrange a day and time the following week. On that day, we would gather the clan in England, they would gather the clan in Canada, then we would all shout "Happy Christmas" to each other. It wasn't until circa 1971 that it became possible to direct-dial international calls.

Today, by comparison, my dear old mom is armed with a smartphone with which she can call me 24/7 ("Oh, I'm sorry dear, I forgot we are six hours ahead of you. It's 9:00 o'clock in the morning here, what are you doing now?").

Technological innovations are coming faster and faster. I can't wait to see what 2024 brings. Whatever comes our way, all of us at DENA will be here to tell you all about it!

Max Maxfield

CLIVE 'MAX' MAXFIELD
Editor, DENA

DENA DESIGNING ELECTRONICS NORTH AMERICA

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ecia Connect. Influence. Optimize.

abc DESIGNING ELECTRONICS NORTH AMERICA IS INDEPENDENTLY ABC AUDITED 2022

TOP STORY

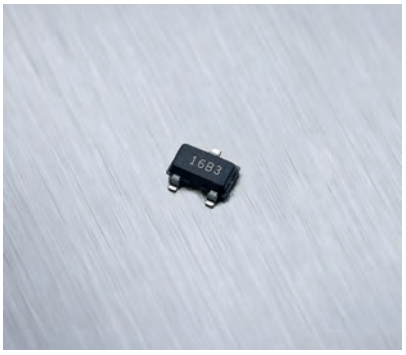
IAR empowers AI/ ML development for Renesas RA8 MCUs

IAR, a world leader in software and services for embedded development, has announced seamless integration of support for Renesas RA8 MCUs in the latest release of IAR Embedded Workbench for Arm. This update provides extensive support for the cutting-edge Arm Cortex-M85-based RA8 devices.

Renesas RA8 Series MCUs are the first to feature Arm Cortex-M85 processors and Arm's Helium technology. With an impressive performance rating of 6.39 Coremark/ MHz, these MCUs are the most potent available today.

The IAR Embedded Workbench for Arm serves as a comprehensive development toolchain renowned for accelerating embedded development while fortifying security.
The combination of Arm's Helium technology and IAR Embedded Workbench's optimization means developers can immediately start building powerful applications in Artificial Intelligence (AI), Machine Learning (ML), and Digital Signal Processing (DSP).

www.iar.com



Melexis micropower switch extends battery runtime for IoT

The growing demand for smart devices to be battery-powered and to last as long as possible is a challenge for the internet of things (IoT). The need for ultra-low-power components that are both reliable and accurate is therefore paramount to the continued development of embedded and connected devices.

To address this, Melexis has announced the MLX92216 and MLX92217 ultra-low-power Hall effect switches. The 1µW and narrower tolerances lead to a predictable power budget, helping to extend battery runtime. These magnetic devices detect open or closed positions. They are ideal for replacing traditional reed switches in IoT, industrial, and white good applications.

www.melexis.com

Cost-effective thin film chip resistors for harsh environments

Thin film chip resistors are increasingly used in modern electronic designs due to their exceptional precision and stability. However, thin film technology is usually more expensive and limited with respect to the power ratings offered.

Stackpole's RNCP series chip resistors utilize high volume thin film technology to provide cost-effective chip resistors that are anti-sulfur per EIA-977 and offer excellent performance and reliability under a wide range of environmental conditions.

www.seielect.com

Integrated display, command input, and application logic

DISPLAY VISIONS combines the input of control commands and the display of measured values or parameters into a single component. The uniTFT smart touch display product range can both receive and output data. With integrated I/O and graphics controllers, users can implement complete small-scale control without additional hardware.

The small-scale controller implements arithmetic and logic operations as well as data communication and storage. The combination of a brilliant color display and integrated touch screen for data input means users can implement countless applications with minimal effort.

www.arkco-sales.com

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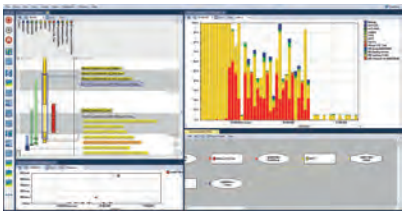

Trace observability for RTOS, middleware, and silicon vendor APIs

Percepio is a leading provider of edge observability solutions for developers of critical operational technology (OT) applications. Percepio Tracealyzer provides trace observability for system-level debugging, verification, and profiling for embedded, edge, and IoT systems. Its advanced visualization and analysis features let product developers speed up development time thanks to 10x faster debugging.

Now, Percepio has announced the immediate availability of Tracealyzer SDK, a software development kit enabling platform developers to create custom observability solutions with Percepio Tracealyzer.

www.percepio.com

Diecast enclosures with built-In RFI/EMI shielding

Robust ROLEC conFORM (IP66, IP67 optional) electronic enclosures are ideal for a wide range of industrial electronics that involve regular inspections and maintenance. Instead of delicate (and expensive) RFI/EMI gaskets that can be damaged by frequent opening and resealing of the lid, a patented tooth system guarantees metal-to-metal contact, thereby creating the conductivity needed to shield the electronics from RFI and EMI. Inside, there are threaded screw bosses for installing PCBs, mounting plates, and terminal rails.

www.rolec-usa.com

IoT proximity sensing with compact reed sensors

Littelfuse has announced the release of its 59001 Reed Sensor. This miniature D-shaped cylindrical device offers compact size, high performance, and customization options, making it an ideal choice for various industrial, appliance, and IoT proximity sensing applications.

The key differentiator of the 59001 Reed Sensor lies in its compact size, measuring just 13.5 mm x 5.0 mm x 4.6 mm (0.591” x 0.197” x 0.181”). The 59001’s small form factor allows for significant space savings, making it ideal for applications where size constraints are a concern.

www.littelfuse.com

KYOCERA AVX components used in lunar mission

On August 23, 2023, the Chandrayaan-3 mission’s Vikram lander cemented India’s spacefaring status as the first country to soft-land a spacecraft near the South Pole of the Moon.

KYOCERA AVX contributed several components to the Pragyaan lunar rover, including stacked TCH Series surface-mount tantalum polymer capacitors, miniature CWR15 MIL-PRF-55365 / 12 tantalum chip capacitors, high-capacitance and low-ESR TES Series ESCC QPL tantalum chip capacitors, space-level TAZ Series/CWR29 MIL-PRF-55365/11 molded tantalum chip capacitors, and high-reliability MLCCs and EMI feedthrough filters.

www.kyocera-avx.com

Magnetic current sensing drives vehicle electrification

by Matt Hein, Product Line Manager, Current Sensors, **Allegro Microsystems**

Magnetic current sensors are replacing sense resistors and current transformers

Modern cars have become increasingly power hungry. Even the "least electrified" vehicles include advanced electronics for infotainment, safety, and engine control. Fully electric vehicles further add high-voltage power domains to charge and drive. Each of these systems shares the need for power monitoring and control, and this is where current sensors are used.

Safety systems and powertrain electrification

OEMs are implementing electrified steering and braking systems to increase vehicle safety and enable automated driving. These systems encompass one or more high-current motors to actuate the steering rack or brake caliper. Safety systems require current sensors to be small and have low heat generation.

A basic electric vehicle powertrain encompasses a charging system and a drive system. A charging system may experience 100A at 400V or 800V, while the drive system may need to deliver several hundred amperes of current to the traction drives. Current sensors require isolation and high current capability, while also operating from DC to a high bandwidth for efficient power conversion and system protection.

Sense resistors and current transformers

Current sensing needs have historically been met using sense resistors and current transformers. The sense resistor (and associated shunt amplifier) provides V=I×R but suffers due to large size, high power dissipation, slow bandwidth, and no inherent isolation. The current transformer provides an isolated, high-speed measurement, but has drawbacks of large component height, no DC sensing, a narrow frequency band, and needing many external components to operate.

Magnetic current sensors bring benefits

Magnetic current sensors are non-contacting sensor integrated circuits. This means the sensor silicon is not touching the conductor carrying the current. Isolation does not require extra components, and ranges from 100V to several thousand volts. The sensor measures the magnetic field generated by the current and outputs a voltage proportional to that magnetic field. Some magnetic current sensors are placed close to a current-carrying wire (with or without a concentrator) while others integrate a conductor path inside the component for ease of implementation.

A magnetic current sensor can provide significant advantages over sense resistors and current transformers in automotive power systems. Compared to a sense resistor, the magnetic current sensor offers a smaller size, lower power dissipation, and higher bandwidth with integrated isolation. Advantages of magnetic current sensors over current transformers are smaller size, DC measurement, and minimal external components.

One example current sensor is the Allegro Microsystems ACS37010, which features 450kHz bandwidth, high accuracy, and integrated reinforced isolation in an enhanced SOIC-8 package. Other solutions such as the ACS71240 are optimized for smaller footprints, with low-or-no-isolation in SOIC-8 or 3x3 QFN packages.

www.allegromicro.com

Micromobility is picking up speed

by Salvatore Potestia, Business Development Manager **& Ralf Hickl,** Product Sales Manager in the Automotive Business Unit, **Rutronik**

Reference designs for 48V low-speed electric vehicles

Low-speed electric vehicles (LSEVs) are ideal for covering short distances in urban areas. Stricter environmental protection requirements such as restricted traffic zones in cities are likely to give these vehicles a considerable boost. Countries with large populations and many densely populated areas, such as China and India, will account for the largest share.

Diversity of micromobility

The term "micromobility" embraces any small, low-speed, electric-powered transportation device used as commercial vehicles or for passenger transportation.

LSEVs include two-wheeled e-scooters, e-bikes, and pedelecs, along with two-, three-, and four-wheeled cargo bikes. The latter are particularly popular with service providers, such as couriers and delivery services, as well as families.

Three-wheeled vehicles include motorcycles with sidecars for private use and small passenger cars, such as the Piaggio Ape. They are suitable for passenger transport, for example in the tourism sector, and are also used by postal services.

Four-wheeled models range from e-quads to small e-cars, such as the Renault Twizy, and small e-vans. Depending on their actual size and design, they are used for a variety of commercial and personal transportation applications.

Performance, speed, and range

Depending on their vehicle class, LSEVs can achieve a range of speeds and power ratings. Smaller two-wheeled vehicles typically have a rated power of 1kW and can reach top speeds of 25km/h. Larger two- and three-wheeled types generally have a maximum power rating of 4kW and travel at up to 45km/h. Low-speed four-wheeled vehicles also travel at this maximum speed; their rated power, however, can be as high as 6kW. Heavy four-wheeled models, on the other hand, can reach top speeds of 90km/h with a rated power of 15kW. The range of low-speed electric vehicles varies depending on their power output; many can travel around 150km on a single battery charge.

Reference designs

Rutronik's Automotive Business Unit (ABU) sees great potential in low-speed electric vehicles. Following the successful reference design for a bidirectional HV switch for 800V DC and 50A, Rutronik is now working closely with Vishay to develop sample applications for LSEVs with a 48V electrical system. These are the on-board charger (OBC) and the traction inverter. Both applications focus on converter efficiency, compact design with low installation height, and automotive-grade quality.

On-board charger

The OBC provides a maximum charging power of 3.6kW. Its key components are the new VS-ENM040M60P power modules, optimized power factor correction (PFC) coils, and a pulse transformer developed specifically for this application. Passive components also play an important role since their properties are a key factor in determining the efficiency of the circuitry. An integrated LLC transformer, such as the MTBB133971 from Vishay Custom Magnetics, is used as the pulse transformer (resonant inductors are already incorporated).

Traction inverter

The traction inverter has a rated power of 15kW with short-term peak power of 25kW. Vishay's N-channel automotive trenchFETs in the PowerPAK 8x8L Reverse Package are used as power semiconductors. Their top-side cooled package allows them to be thermally coupled directly to a heat sink rather than being cooled by the PCB.

Summary

LSEV reference designs provide hardware developers with design templates that can significantly reduce the time-to-market of their own circuit designs. By using the latest high-performance components, these circuits achieve high power density at low cost.

www.rutronik.com

Image: Scharfsinn/Shutterstock

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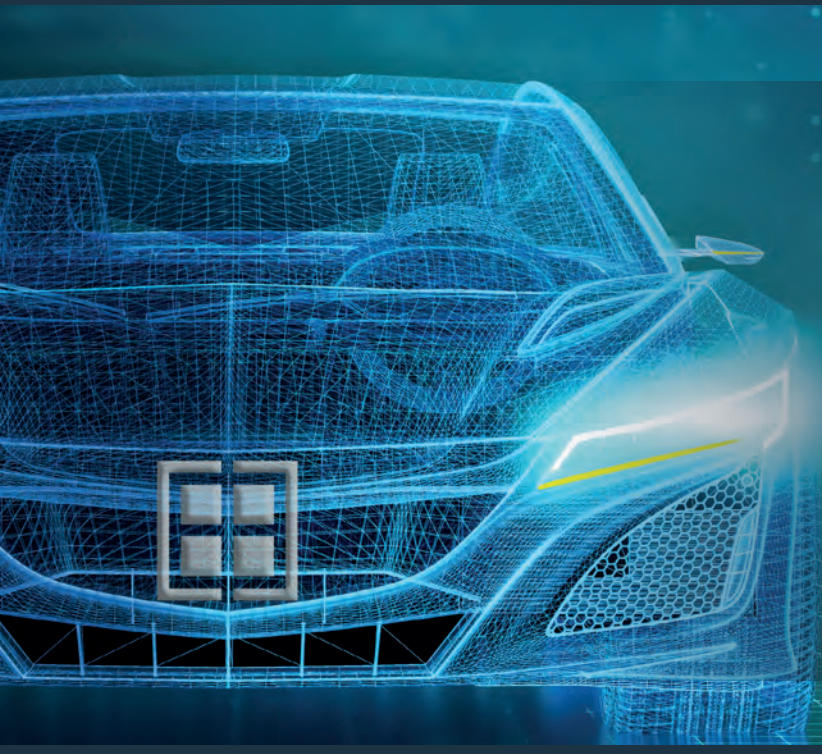

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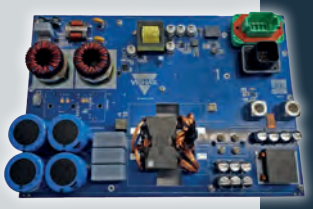
NEW ELECTRONIC REFERENCE DESIGNS

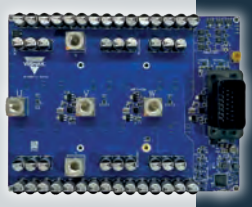
On-Board Charger (OBC) 48V

- 3.3KW power class
- Silicon Power Modules
- Combination of several modules
- EVSE interface (Charging)



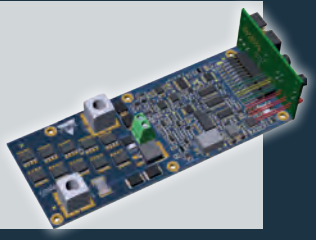
Inverter 48V

- Integrated temperature sensor
- Power value up to 25KWp
- Top Side Cooling and Low RDS(on)
- Shunt-based phase current measurement



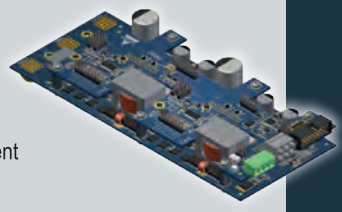
eFuse

- Voltage measurement up to 60V
- Switching current up to max. 100A
- Pre-charging and high over-current protection
- Passive cooling



48V/12V DC/DC Converter

- Bi-directional usage
- Power of up to 1KW
- Integrated voltage, current, and temperature measurement



800V/50A HV-Switch

- Stand-alone or BUS operation
- 1200V SiC-MOSFETs
- Adjustable over-current threshold
- Fast massive over-current turn-off (~2.5µs)
- Optimized thermal design → passive cooling

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ecia MEMBER

Overcoming electric vehicle adoption challenges

Gabe Osorio, Director, Transportation Marketing, **TTI, Inc.**

Power management systems will play a key role in the culture shift to EVs

The shift to electric vehicles (EVs) has turned out to be anything but an overnight revolution. Even as the charging infrastructure expands, sticker prices come down, and sales go up (from 5% of all new cars sold in 2020 to 14% in 2022), we're still adapting one piece at a time.

This shouldn't come as a surprise, of course. The first modern interstate highway, the Pennsylvania Turnpike, wasn't opened until 1940, more than three decades after the launch of the Model T Ford in 1908. Meaningful change is never instantaneous.

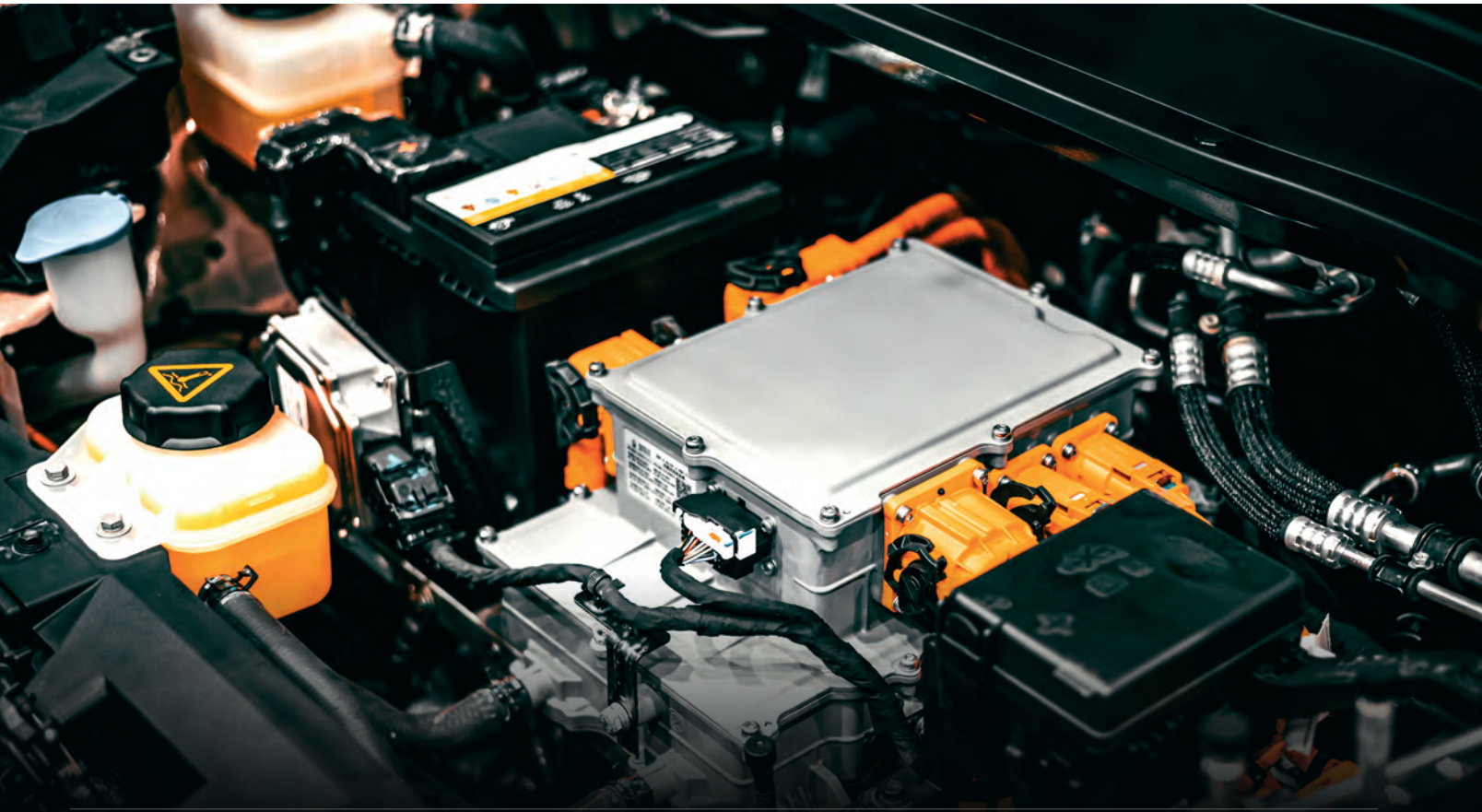
We're getting there, but according to a Yahoo finance survey, just 40% of millennial-aged drivers report a willingness to buy an EV, and that number gets lower and lower as you go back through each generation. This survey also reports that 70% of those polled had never been inside an EV in the first place.

That even the youngest car buyers are hesitant to get on board should stand as evidence that some of the biggest hurdles the EV industry faces are cultural.

Normalizing the EV

Generally speaking, all the right numbers are ticking up, and there will be an eventual tipping point where the EV has been totally normalized, wherein the novelty wears off. EVs will become "just another option" and—from there—the preferred option.

Tesla continues to lead the market, reinforcing the impression of EVs as a status symbol despite a long list of practical advantages over conventional vehicles, including lower maintenance and fuel costs.



To persuade more drivers to consider an electric vehicle, EVs need to be presented as a practical alternative to conventional autos, and fleet use stands at the front line of this change.

There are plenty of reasons for fleet managers to consider EVs. In California, the standard mileage reimbursement rate stood at around 0.655 cents at the end of 2023, up from 0.585 cents in January 2022. That may not sound like a big spike, but when you consider that the reimbursement rate was the same in 2022 as in 2008, even this small increase points to trends that fleet owners need to keep an eye on.

On average, drivers can expect to get three to five more miles out of a gallon on the highway than they do in the city, so anytime gas prices see a spike, it will be the last-mile delivery services, couriers and transportation companies that feel the pinch first, with the constant stop-start rhythm of making deliveries in the city.

A cycle of improvement

It is difficult to blame delivery, transportation, and courier companies for hesitating to switch to an all-electric vehicle fleet. For every plus to converting, there's a minus.

The San Francisco area boasts more than 14,000 EV charging stations, Los Angeles nearly 20,000, and the state of Vermont leads the pack, per capita, with one EV charger for every 703 residents. That's all good for companies in these areas, but in rural areas and small towns from coast to coast, it's not difficult to drive a hundred miles without seeing a single charging station. In Mississippi, for instance, you'll find just one charger per ten thousand residents.

Thankfully, solutions are already underway. Federal funds to the tune of $7 billion for EV battery components and materials and $7.5 billion for EV charging infrastructure have been allocated in an effort to achieve net-zero emissions by 2050.

What we should expect to see in the coming years is what we tend to see whenever a new technology rolls out: The technology is first championed by a niche group until the infrastructure is built, encouraging more investment into the hardware, which enables greater investment into the infrastructure, and so on. Through this cyclical process, as technology improves, it becomes more affordable, efficient, reliable, and accessible.

Bold but cautious steps

For every example of a business owner who lost out through hesitancy to adapt to changes in their field, there are just as many examples of businesses sinking their resources into hasty, ill-conceived changes in direction.

For instance, selecting a subpar inverter for transforming Direct Current (DC) to Alternating Current (AC) comes with risks like heat runaway. This positive temperature feedback effect causes components to overheat due to insufficient cooling through battery walls. If you've ever seen a device melting at the charger port, you're probably looking at an instance of heat runaway.

When it comes to the motor driver—the component used to manage vehicle speed and torque—you have your usual issues like overheating, as well as any number of potential compatibility hangups. In particular, software issues head the most common problems reported by fleet owners.

Building effective power management systems is key to the coming shift to the EV era. Effective, efficient power management means fewer hazards, safer vehicles, less strain on the charging infrastructure, and further proliferation of electric vehicles, bringing us ever closer to that inevitable tipping point.

The motor driver also manages the actual driving experience behind the wheel of an EV. With multi-gear shifting and effective torque management, you have an electric vehicle that's easy and intuitive to drive.

New horizons

These are uncharted waters for many business owners. If you are investing in electric vehicles at any level right now, you are an innovator, which comes with a certain degree of risk. But that doesn't mean that the inherent risks to innovation can't be managed and mitigated.

Ensuring that you're working with the right people is critical to moving with confidence. A fleet owner's job is to manage their fleet; expecting them to become an overnight expert in EV parts distribution is simply unrealistic. Beyond simply selecting the right components for a power management system, supply chain issues need to be considered, including component availability and cost considerations. This is why finding the right distribution partners in the EV field is so important.

"Effective, efficient power management means fewer hazards, safer vehicles, less strain on the charging infrastructure, and further proliferation of electric vehicles, bringing us ever closer to that inevitable tipping point."

TTI is devoted to facing new challenges in the EV field head-on, relying on our network of seasoned transportation specialists to keep their fingers on the pulse of new market and technological trends to secure the right components at the right price for optimal performance. We're proud to have shipped more than 27 billion units in the last year alone, setting an industry-leading delivery rate and ensuring that our partners have everything they need to stay on the cutting edge of their own respective industries.

www.ttiinc.com

5G-based LEO satellites will grow IoT adoption

Tomer Yablonka, Director of Cellular Communication, **CEVA**

There is growing appetite for standards-based 5G LEO satellite cellular

When most of us think about widespread technology adoption, we have a pronounced urban bias. Tech growth pitches around 5G are based on emerging applications in western cities and progressive adoption in urban areas in developing countries. Beyond that, most pitches get a bit fuzzy. On-the-ground IoT applications are clear—soil humidity and temperature sensing, for example—but how these communicate with a datacenter is less clear.

Line of sight 5G base stations are available only where there is enough demand (generally a nearby town) to justify the cost of a base station. And, even then, only in relatively clear areas; forested or mountainous regions, oceans, or deserts need not apply. Mesh networks and fixed wireless access can expand the reach to IoT devices a little around a base station but still under the same restrictions. In contrast, low earth orbit (LEO) satellite options like Starlink are visible everywhere they are deployed but depend on proprietary protocols and hardware link support. It is not surprising, therefore, that there is growing appetite for standards-based 5G LEO satellite cellular to truly open up this market.

Satellite options

Satellite support for phone communication is not a new idea. Motorola introduced their Iridium system in the 1990s. The first generation was not successful probably because we weren't yet ready for that level of coverage, and emerging cellular solutions were more effective and lighter weight (I should note in fairness that a newer version of Iridium is active today). Now that cellular is ubiquitous (at least where coverage is available), many feel it is time to revisit the satellite option.

There are three orbit options: geostationary orbit (GEO), middle earth orbit (MEO), and low earth orbit (LEO). GEO orbits at ~35,000km and offers the advantage that any given satellite is always at the same position in the sky. This works well for high bandwidth home-based communication for TV and internet service in remote areas. Here, a dish can be aligned once with a satellite and does not need tracking support. HughesNet is one service that offers this option.

MEO satellite orbits lie between 2000km and 35,000km and are mostly used for positioning systems such as GPS and GNSS, also for moderate bandwidth support in remote areas. LEO satellite orbits lie between 160km and 2000km and are the hot option for 5G (and beyond) communication. However, both MEO and LEO satellites move relative

to a user, requiring added support to maintain a link.

GEO satellites are big, costly, power hungry (to communicate over a long distance), and expensive to launch. MEO and LEO satellites are progressively smaller, cheaper, less power hungry, and cheaper to launch, especially considering the advent of small satellites (SmallSats). Also, MEO and LEO satellites can provide better coverage at high latitudes. Each provides unique advantages and disadvantages, suggesting a blend of options may be ideal for satellite-based communication.

Market opportunity

This is an early-stage market but backed by some heavy hitters. Starlink stimulated early visibility, Amazon has its Kuiper project, T-Mobile is working with Starlink and with OneWeb, and there is talk of Google collaborating with Verizon. Market forecasts are very encouraging—$29B by 2030 with a CAGR of 29%—which makes sense. How else would we build a truly worldwide communication infrastructure, not just "worldwide as long as you are in/near a city, not in the mountains, not in a forest, not at sea far from a port, not…"?

In our modern and riskier world, those limitations are no longer acceptable: wildfires, hurricanes, flooding, and crop failures pose risks that 5G satellite-based IoT technologies could help mitigate if deployed widely. Critical services, such as emergency communications for individuals or emergency services, should be able to continue to function even if power is lost. This becomes possible if emergency communications from user equipment (UE) to a dish/ feeder station can connect direct to a satellite.

Of course, we want competition to drive prices down and accessibility, quality, and capabilities up. That can't happen if we are locked into Starlink or a similar proprietary service. This is why we need a 3GPP-ratified standard with which all infrastructure and UEs will play nicely.

Technology challenges

LEO satellites present a terrific new communication opportunity both commercially and for society in general. Nevertheless, there are new challenges that come with these satellite-based systems. One is latency. Latency to a

geostationary satellite can be 600ms versus 30ms for a cable signal. That may seem high, but it isn't just simple round-trip time. There's a lot of other processing going on too. LEO satellite latencies fall in the range of 180ms, which is better than the geostationary option, but still quite a bit longer than ground-based communication. These latencies are not currently suitable for ultra-low latency applications, but for many IoT uses such a latency may not be a problem.

While a LEO satellite orbit improves latency, it also covers a smaller area at any one time and is moving (multiple orbits per day) demanding frequent communication handovers between satellites, even when the ground UE device is stationary. Handovers add some of that latency to communication. Link controllers may choose to handover to another LEO satellite or perhaps to a nearby MEO satellite offering a longer period before the next handover. Unsurprisingly, algorithms in this area are continuing to evolve.

An additional problem comes from Doppler effects. To stay in orbit, LEO and MEO satellites must move quickly, MEO satellites at 3.1km per second (km/s) or more, LEO satellites at 7.8km/s. Doppler shifts at these speeds can be severe, especially for LEO satellites, and that shift can significantly degrade link reliability. Corrections based on the known ephemeris of a satellite are effective only if the ground terminal is stationary or at least has predictable movement, which is typically not the case.

Alternative modulation schemes have been proposed that can compensate for Doppler, such as OTFS (orthogonal time frequency space) rather than a more conventional OFDM (orthogonal frequency division multiplexing). Other methods propose deep learning as a method for compensation (when connecting to dishes rather than a movable UE I would guess). Once again, this is an area where algorithms are evolving quickly.

Network implementation

Start with the 5G network architecture. There are different architectures proposed for different use-cases. One offers a direct connection between an IoT device and a 5G LEO satellite in the service link while the satellite connects with the core (terrestrial) network through a feeder link provided by a satellite dish. Another architecture has the same setup for the feeder link, and a service link from the satellite also connects through a dish which in turn connects to an edge network, say for 5G fixed wireless access.

Standardization through 3GPP is still underway, though they are already suggesting the possibility of tens to hundreds of Mbps bandwidth (with a dish) in the downlink and roundtrip delays on the order of a few tens of milliseconds, all subject to multiple factors of course.

Clearly, between handover management and Doppler mitigation plus methods to minimize latencies for different classes of service, new hardware and software will be required. UEs supporting direct satellite links will need enhancements, service and feeder link hardware must be provided, and the satellites themselves must support the protocol, all as those protocols evolve.

Demands on HW/ SW development

Already with Open RAN there has been an accelerating trend away from off-the shelf CPUs, FPGAs, and DSPs. Infrastructure and user equipment makers want to maximize differentiation and minimize capital and operational costs. This trend will be further amplified for satellite-based networks. Off-the-shelf products are too costly and power hungry with limited differentiation options to appeal to OEMs. In this area, OEMs will turn even more to ASIC-solutions with software-defined radio (SDR) architectures. This will be essential to enable future proofing in anticipation of algorithm upgrades discussed earlier, as well as to support a wide range of existing and future service opportunities to further differentiate products.

From my perspective, these requirements suggest that any competitive solution must offer the following characteristics as an embeddable IP with strong hardware acceleration options yet significant software configurability:

- For Open RAN implementations, the full range of Open RAN support in the base station (supporting both Macro DU and virtual DU as well as Small Cell capability) and in the radio (supporting Open RAN Low-PHY, Massive MIMO and Beamforming).
- For the UE, a baseband platform with a modem supporting the full range of 5G eMBB, URLLC, Sidelink, and RedCap use cases, for both mmWave and sub-6GHz, as well as legacy LTE and Cat 1 technologies. This embedded IP also should offer configurations to support high-end use cases (such as V2X automotive applications) as well as low margin, ultra-low power use cases (such as agricultural monitors).

On top of these use cases, as the 3GPP definition moves towards standardization, the solution must offer significant software-based flexibility in ability to evolve the SDR algorithms.

At CEVA, we have considerable experience in offering a wide range of wireless platforms, especially cellular options, already proven in 5G, building on our Open RAN platform, and—for baseband applications—building on our 5G Modems platform. We are tracking this domain very closely and would be happy to share our ideas.

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Preparing for the quantum era

by Mamta Gupta, Director of Marketing Security & Comms Segment, **Lattice Semiconductor**

Organizations must prepare for post-quantum cryptography (PQC)

Welcome to the quantum era. While once considered a distant prospect, experts now estimate that the first fully error-corrected quantum computers could be here as soon as 2030. A cutting-edge innovation that combines computer science, physics, and mathematics, quantum computers signal a monumental leap forward into uncharted technological territory.

However, as quantum computing emerges on the horizon, it brings with it unprecedented challenges for the cybersecurity landscape. Most prominently, many of the security controls used today are incapable of defending against quantum-based attacks. Quantum computers will break the cryptography that is central to cybersecurity, intensifying existing risks and creating avenues for new threats. Further, due to quantum computing's superior computational power, various cryptographic algorithms could be rendered obsolete soon. In fact, some experts believe that Y2Q—the time when Quantum computers will break classical asymmetric crypto—is only about 10 to 15 years away. In addition to quantum computers' ability to break existing cryptographic security measures, we're also seeing Steal Now Decrypt Later attacks transpiring today, where bad actors are harvesting encrypted data and storing it to decrypt with quantum Computers later.

While quantum computing will undoubtedly transform key industries for the better, its cyber threats demand our immediate attention. Organizations must gear up to revamp their information security systems to be Quantum Resilient. Regulators are moving aggressively to ensure that critical infrastructure is protected against these threats. But with everything from doorbells to cars connected to the internet, the overhaul of the security of these systems will take a long time.

Quantum computing amplifies cyber threats

Utilizing specialized hardware components and algorithms that leverage quantum physics, quantum computers will outpace current supercomputing technology. For example, quantum computers built by the University of Science and Technology of China can perform calculations at ten million times the speed of the world's fastest supercomputers.

While this newfound speed might seem like a good thing, it also means quantum computers can quickly and easily bypass security measures intended to safeguard systems and data. Specifically, quantum computers leverage Shor's Algorithm to rapidly decipher public key infrastructure (PKI) based algorithms, the typical algorithms used to protect most of today's classical computing systems. Current security standards—like Trusted Platform Modules (TPMs), IEC 62443, and ISO/SAE 21434—all use PKI-based algorithms and, therefore, are not equipped to defend against incoming brute force quantum computing attacks. This leaves

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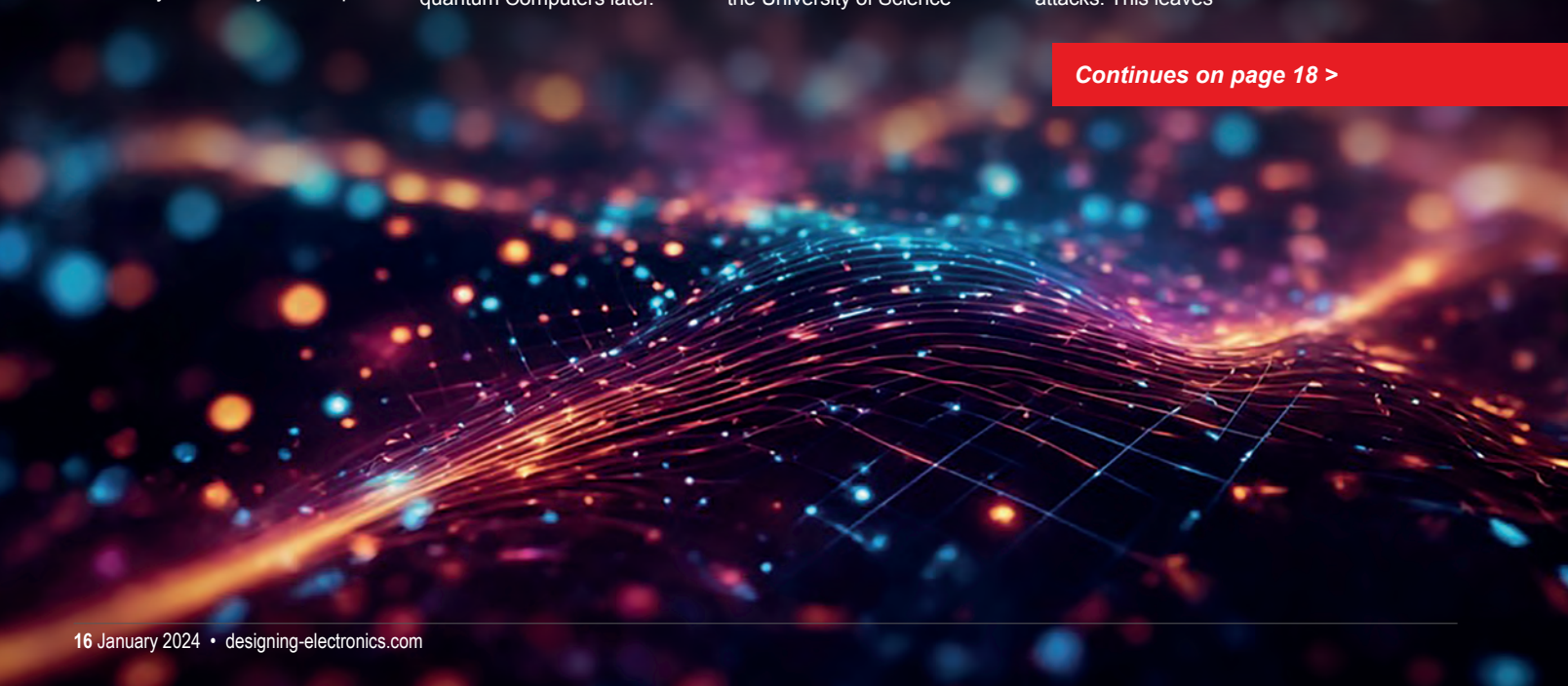
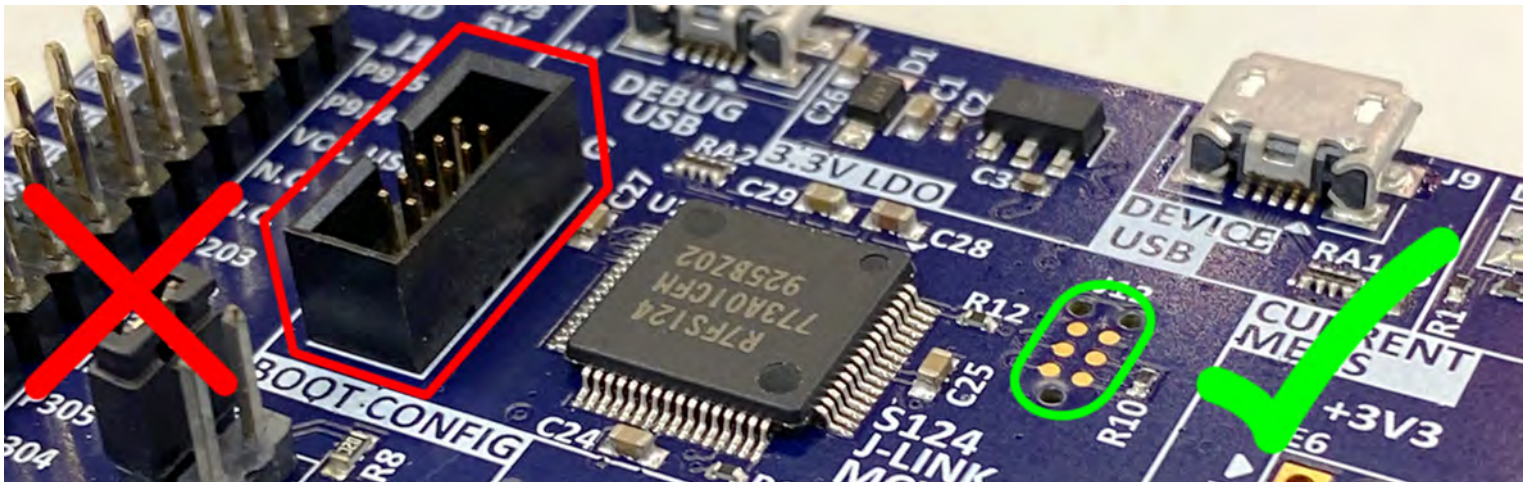


Tag-Connect



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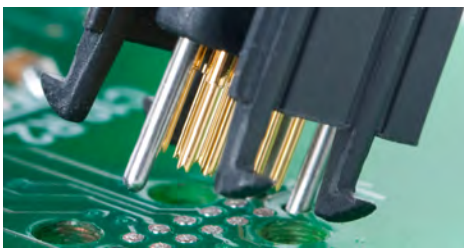

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organizations ill-equipped to face the coming quantum computing challenges.

With quantum computing rapidly approaching, new quantum-resistant solutions, like post-quantum cryptography (PQC), are urgently needed to protect critical infrastructure. PQC adoption is a shift away from the legacy PKI cryptography we see today to more resilient algorithms that are resistant to quantum computer attacks. The U.S. government has even expressed the need for accelerated PQC adoption. Recently, President Biden signed the Quantum Computing Cybersecurity Preparedness Act, making it clear that organizations must adopt PQC as soon as possible to maintain resilience in the face of this new threat.

Fortunately, there are solutions already available to help streamline PQC migration and ensure a secure post-quantum future.

Preparing for a post-quantum world

Organizations should be focusing on implementing a PQC readiness roadmap to prepare for post-quantum era attacks. NIST announced four candidates for standardization in 2022 but they will not be finalized until 2024. Having a plan in place that clearly outlines how PQC will be integrated once available is key. To emphasize the need even further, NIST, CISA, and the NSA recently encouraged organizations to develop PQC readiness roadmaps.

Implementing this roadmap and getting on board with PQC as soon as possible is critical considering the Steal Now, Decrypt Later stance many threat actors are adopting. So far, two algorithms, XMSS and LMS, have released final versions and are moving towards addressing the new and stringent CNSA 2.0 requirements for PQC.

In addition to developing a PQC readiness roadmap, organizations must have the necessary tools to implement PQC once the algorithms are finalized. Field Programmable Gate Arrays (FPGAs) are the best tool for this as they can help facilitate PQC migration as part of a post-quantum readiness roadmap.

Some of the latest FPGAs contain “crypto agile” capabilities that deliver upgradeable protection. Their flexible programmability and parallel processing functions enable developers to easily update existing systems and hardware with new PQC algorithms for adherence to evolving standards. Further, some FPGAs contain Hardware Root of Trust (HRoT) functionality that ensures the protection of platforms and other connected device applications to safeguard an organization’s attack surface. Lastly, FPGAs accelerate complex mathematical functions to enhance system performance and protection.

Building a secure PQC future

Quantum computing has great potential to revolutionize our world—both positively and negatively. While we’ll see advancements in healthcare, finance, and other industries, the technology also possesses the ability to dismantle cybersecurity as we know it.

To navigate the rise of quantum computing, organizations must be committed to the proactive adoption of PQC to secure our systems, data, and infrastructure. Developing PQC readiness roadmaps becomes imperative, providing a structured approach for the integration of the new algorithms once finalized. Further, FPGAs emerge as indispensable tools in this transition, offering flexible programmability, enhanced protection, and the capability to adapt to evolving standards.

As we move into the quantum era, organizations hold the key to a secure digital future. With PQC, we can effectively safeguard against quantum-powered threats and ensure the resilience and security of tomorrow’s digital landscape.

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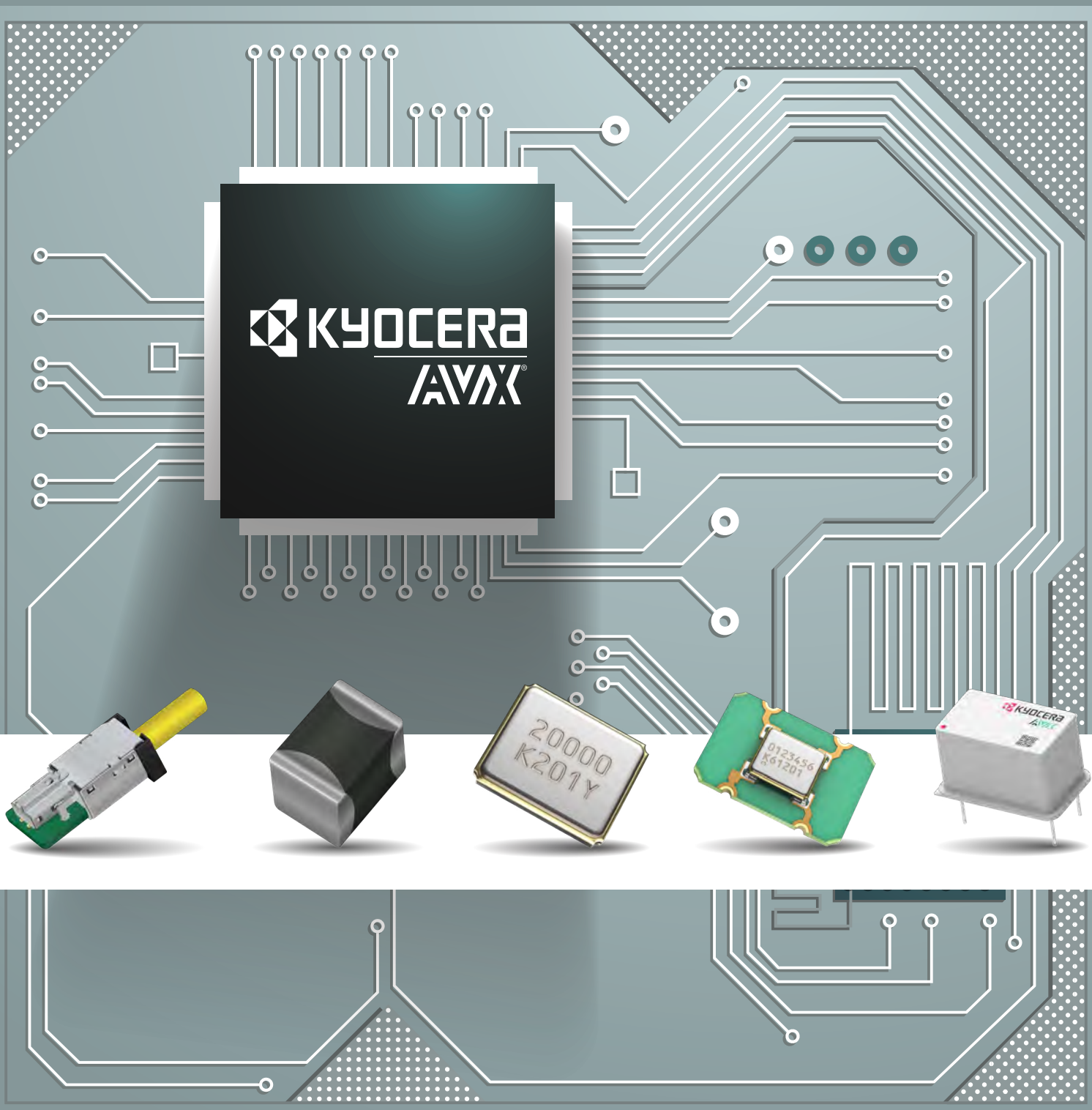
“In addition to developing a PQC readiness roadmap, organizations must have the necessary tools to implement PQC once the algorithms are finalized.”



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The evolution and future of semiconductor IP interconnect

Ravi Thummarukudy, CEO, **Mobiveil**

Interconnect technologies are the backbone of SoCs, including the emerging chiplet market

The evolution from the early days of reusable semiconductor intellectual property (IP) blocks built by a couple of engineers in a garage to a $4.5-billion or so market segment has been a remarkable feat. While the growth, customer success, and economic impact of the processor IP market with companies like ARM, MIPS, and CEVA are well detailed, often overlooked is the contribution of interconnect IP and the network of connections that made it possible.

The IP business came about because of standardization, evolving from circa 2000 to 2010 when it became a business with third-party, pure-play IP companies. As soon as protocols were standardized, startups appeared offering PCI (and later PCI Express), USB, and memory controller IP blocks. Primarily EDA-only companies like Synopsys and Cadence realized that their customers would also outsource IP and look for dependable vendors to provide it. And so, they started acquiring IP startups and later extended their IP portfolios by internal development or more acquisitions. This is how the interconnect IP market came about.

Interconnect IP is today a healthy and growing market segment, a subset of the overall IP market, often referred to as the unsung hero because it doesn't get as much attention as the processor/DSP IP market. Yet, IP interconnects are equally important components in the design of system-on-chip (SoC) devices and peripherals for interconnect. These interconnects integrate onto one SoC all the major functions that were traditionally separate, discrete chips on a computer or networking motherboard. Minimizing external components onto one SoC reduces size and cost and increases yield and efficiency.

A look back on IP interconnects reveals the evolution of standards such the Universal Serial Bus (USB), which was unveiled in 1996, PCIe, which was introduced in 2003, and Computer Express Link (CXL), which rolled out in 2019. Other protocols like Hyper Transport, RapidIO, Gen Z, CCIX, and OpenCAPI targeted specialized markets and applications. For example, RapidIO was successful in the wireless and industrial markets and later in high-reliability automotive and aerospace applications. Gen Z focused on optimized storage applications, while CCIX targeted accelerators. However, the lack of processor companies supporting these interconnects caused them to fade away, leaving PCI Express, USB, and others to dominate the market.

A view of the future reveals a growing demand for data-intensive artificial intelligence (AI) and high-performance computing (HPC) applications driving a need for high-bandwidth chip-to-chip interconnect technologies such as the Universal Chiplet Interconnect Express (UCIe), which was unwrapped in 2022.

The early days

Every chip design team had a small repository of designs and utilities shared and reused across multiple projects. Typically, these blocks of code were never fully documented, and support meant calling out across the cubicles to another engineer with knowledge about these legacy designs. Sharing IP and information across companies today is a well-accepted and proven methodology. Every semiconductor company has a centralized IP enablement team that maintains internal and external IP as well as providing support to various SoC design teams. Just like EDA procurement, IP acquisition has been centralized due to technical and economic factors.

In the late 1990s, typical systems were comprised of many different standard semiconductor chips like a CPU, a DSP, and memory interconnected on a PCB. Advancements in VLSI integration made it possible for more transistors on a single silicon die. This led to the integration of CPU and DSP Cores along with other higher-level functions and memories on silicon, which became SoCs. One of the earliest examples is the LSI Logic I/O processor chip developed for the Sony PlayStation-II design. As part of this, a set of tools and methodologies was developed for IP core-level integration and verification, which became the blueprint for similar complex SoC designs.

As an individual chip's complexity increased, so too came an increasing need for data to be fed into it. Having different chips with different I/O protocols and electrical characteristics

became untenable and led to interconnect standardization. The first generation of interconnects were slower and needed many pins. As complexity increased, the data bandwidth also needed to be increased while using fewer pins, leading to the development of high-speed serial interconnects in the early 2000s.

This form of IP interconnect became a foundational element for SoC success. The interconnection had to be sophisticated because the data was complex and needed error correction among other things.

Today, there are a variety of interconnect standards such as Ethernet, PCIe, and PCI Express. Over time, high-speed serial interconnects became popular for fewer pins and high-speed, high-bandwidth data transfers. From Generation 1 to Generation 6, speed and bandwidth multiplied. All these technologies and their five or six generations of standards found their niche in terms of where each can be applied.

Early on, USB was consumer-centric and became the consumer-friendly interconnect for PCs, laptops, and so on. USB was everywhere, even for storage with USB dongles, and it is available now for every kind of application. It's also one of the easiest interconnects to use as plug-and-play (plug it in and it works). This is a great success showcasing companies coming together to create a standard and implementing their own version of this standard. PCIe was yet another IP standard that became popular in the compute, networking, and storage markets.

A new standard

While the aforementioned interconnects are outside the chip, there are also interconnects inside the chip, such as Arm's AMBA, which includes the AXI and CHI protocols, for example. Inside the chip, there are many interconnected components connected through a standard fabric, which is referred to as the SoC fabric. The AMBA specifications are interconnects inside the chip. Outside the chip are the high-speed serial interconnects like PCIe, USB, and so on.

The new CXL standard extends PCIe connectivity and provides a pooling capability to share memory between chips. A data center architecture demands pooling or sharing of coherent memory between the CPU, GPU etc. so that every chip can read/write to the main memory coherently.

CXL enables a design to attach additional memory via PCIe. This is not as fast as the main DDR memory, but it's available as an expanded memory through the CXL protocol.

The critical importance of standards

IP interconnect standards and their evolution are maintained and managed by industry standards consortiums comprised of big and small companies responsible for specifying open protocol specifications. Company representatives help set the standard and collaborate to ensure that standards are maintained, updated, and meet the needs of the industry.

Consortiums are structured in such a way that there are big companies who have the market need and muscle and budget to allocate additional resources to become the promoters. Big and small companies participate and contribute.

Adopters use the technology without contributing. Students, consultants, and universities are another class of membership.

Many participating companies share their patents through the consortium to further a collective effort and level the playing field so all companies can make use of the standard without worrying about patent infringement. This is important because otherwise legal issues could ensue and slow adoption.

Apart from the specifications, these consortiums facilitate compliance and interoperability of standards interpreted by individual companies. They produce an interoperability requirement and certify it with their logos. Companies go to USB, PCIe, or Ethernet compliance labs to run tests that prove interoperability with the different chips resulting in a logo certification.

The industry consortium structure certainly helped move the market driven by needs, such as growth in internet, storage, data centers, and on-line shopping. Companies dropped their proprietary connectivity methodologies and adopted third-party, industry-wide standards.

Sure, the 600-pound gorillas of the market can still afford to have non-standard interconnects. Nonetheless, the industry needs standards consortiums because these collective efforts propel the market forward. The IP business itself is huge and its evolution is healthy and growing.

The emerging chiplet market

Standards consortiums create collaboration when the chip industry participates, and they will play a big role as SoCs evolve to chiplets and new interconnect standards emerge, such as UCIe.

Interconnect technologies are the backbone of SoC designs, including the emerging chiplet market. As monolithic chips become bigger and more complex, high yield becomes increasingly difficult. Building the whole chip becomes cumbersome and unwieldy, and few companies can afford it. The economics say to split the chip into blocks called chiplets, then stack them together into an application chip or 3D IC packaging.

Chiplets are a timely solution because of the slowing of Moore's Law and increasing costs. That's where the UCIe standard helps grow the ecosystem. Chiplets will require vendors to employ a standard interconnect that allows a chip design company to stitch them together. It is not easy to put multiple chiplets together in a 3D integrated chip. Skills are needed, and standards will help this industry move forward and build an independent standard chiplet market segment.

In theory, it's great to have standards-based chiplets. In practice, it is not that straightforward. A chiplet strategy depends on another company's chiplet that needs to be integrated and verified. Unlike SoC designs, verifying 3D ICS are much more complex and this issue needs to be resolved fairly quickly for the market to flourish.

Certainly, this industry must progress further before using third-party chiplet IP becomes a standard practice. The future of large semiconductor development is based on 3D ICs with many chiplets from internal and external sources. That is the next step. The industry is not there yet. UCIe is a step forward.

Conclusion

Interconnect standards and IP played a critical role in the adoption of SoC design methodologies enabling the acceleration of the development of electronic products. Industry consortiums led the way.

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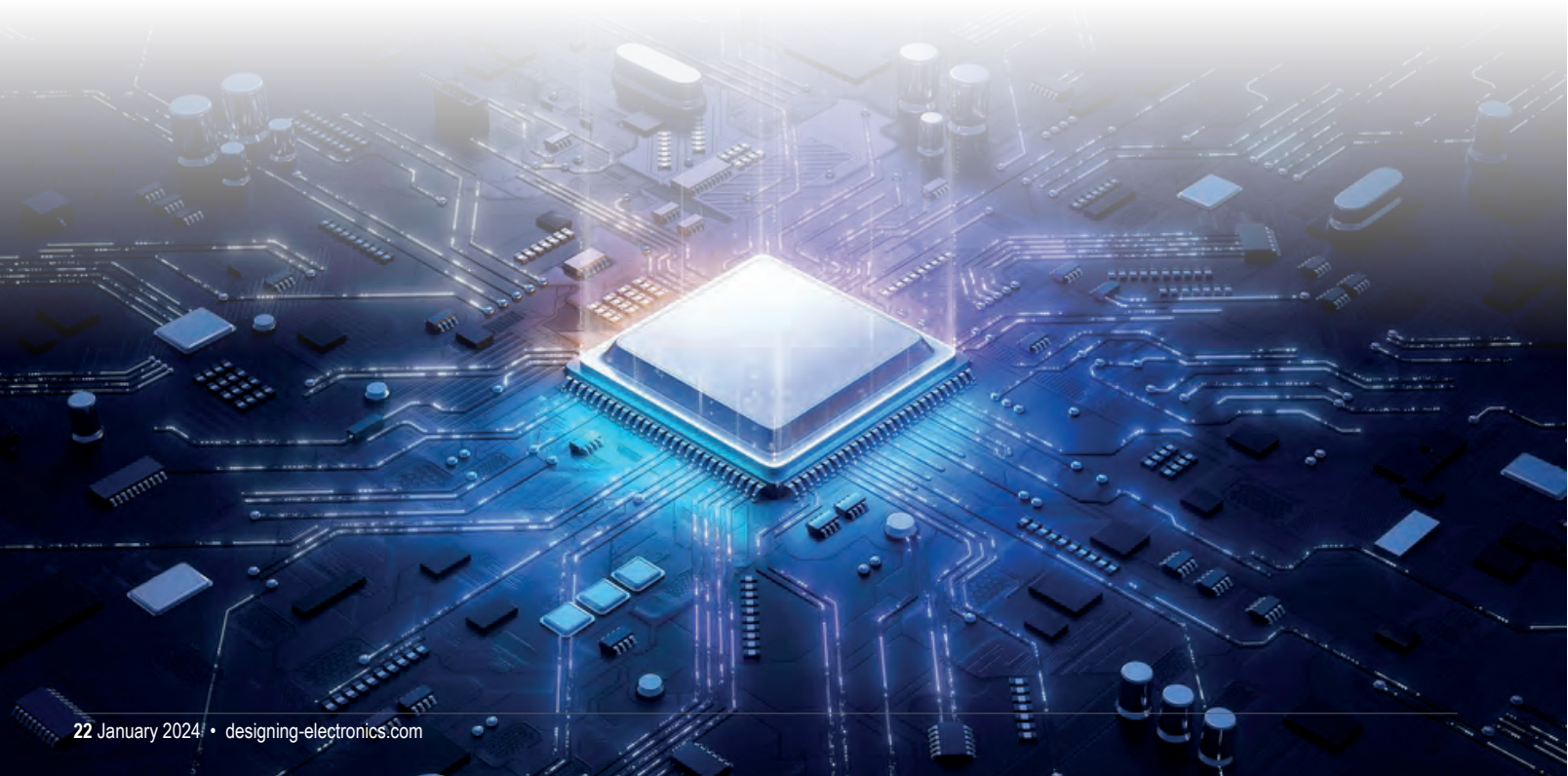

Modern techniques for testing embedded software

Get more done in less time and on smaller budgets

Jacob Beningo, President,
Beningo Embedded Group

Testing embedded software and firmware can be tricky. Traditionally, embedded software is tightly coupled to hardware, which makes testing software without the hardware challenging. The rising complexity of embedded systems and the demand for an ever-growing feature list have made quality—specifically testing—a significant issue. Teams can leverage several modern techniques to ensure their embedded software is testable.

Hardware abstraction layers

Developers can ensure testability and portability across different hardware platforms by decoupling the application code from the hardware. A cornerstone of modern embedded software testing is the implementation of a hardware abstraction layer (HAL). This acts as a bridge between the software that interacts with the hardware and the higher-level application code.

Consider an embedded system responsible for sensor data processing. The HAL would provide a consistent interface for sensor data acquisition, regardless of the underlying sensor hardware. This allows testers to inject simulated sensor data through the HAL for testing the processing logic without needing the actual hardware sensor. The result is a more flexible and efficient testing process that can be conducted early and in parallel with hardware development.

Unit test harnesses

Once a team has a good hardware abstraction layer, they can more readily unit-test their application code. Unit testing is a methodology where individual units of source code are tested to determine whether they operate as expected. Teams can use many open-source and commercial tools, such as CppUTest, Unity, GoogleTest, etc. These tools allow developers to verify functionality and track their test coverage. For example, CppUTest provides a simple platform for writing and running unit tests in C and C++. It includes features such as memory leak detection and minimal platform dependency, which are particularly useful for resource-constrained embedded systems.

Automate test workflows

Continuous integration and continuous deployment (CI/CD) pipelines allow teams to run their tests continuously and identify issues. These tools automate the process of building, testing, and deploying software, ensuring that every change made to the codebase is verified. Automated verification includes running a suite of tests ranging from simple unit tests to complex integration and system tests. These tests can be run with every code commit, every merge, and even nightly to ensure nothing has gone amiss.

Modernize your testing

Leveraging modern testing techniques is essential with the demand to get more done in less time and on smaller budgets. To succeed, you must have well-defined HAL, unit testing, and test automation processes. Each of these elements plays a vital role in ensuring that embedded software meets the highest quality and performance standards. As the field advances, these testing techniques will become ever more integral to the development lifecycle of embedded systems.

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Making satellite connections

Choosing connectors to address the challenges facing NewSpace satellite designers

Recent years have seen the emergence and the rapid growth of the so-called 'NewSpace' sector as private enterprise continues to expand its presence in the potentially lucrative businesses of everything from space tourism to commercial communications and asset tracking. According to market intelligence firm Euroconsult this market grew by 8% last year and is expected to reach over $737B within a decade. Much of that growth will come from developing the satellites needed to deploy many of the new and emerging space-based services.

Thanks to the unique environment in which they operate, electronic systems for satellites present engineers with additional challenges over and above those they face when developing applications for use on Earth. Among these are operation in a vacuum and at extreme temperatures, protecting against radiation, and delivering rugged solutions that must function reliably for many years.

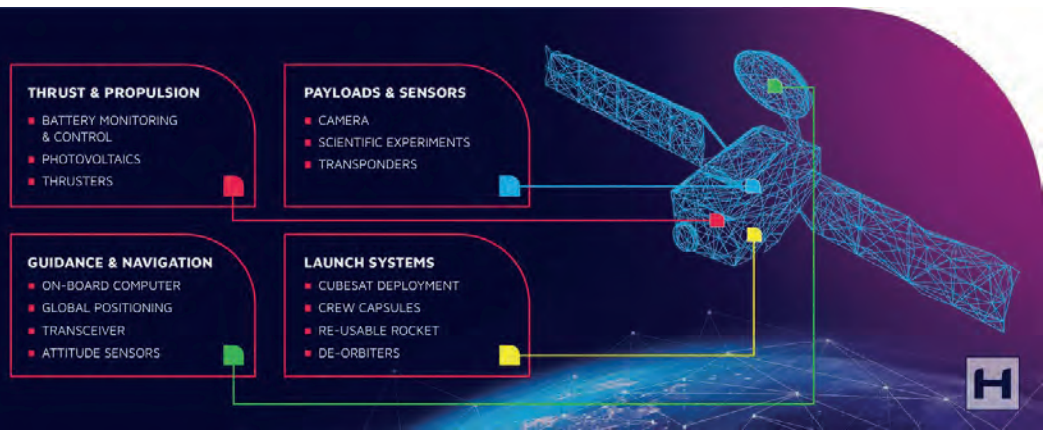
While several standards have been created to certify the reliable operation of space-grade components, qualification to these standards is typically a lengthy and expensive process. This is out of step with the pressures that today's NewSpace satellite designers face to optimize performance and minimize time-to-market to maintain competitive advantage and ensure commercial viability. Of course, these designers still need to pick products that are tested to the relevant standards for space, but they do not necessarily want to be restricted to choosing only those with official certification as this can lead to prohibitive cost models at the same time as limiting access to the latest technologies.

Connector selection

The challenge of creating robust system architectures in satellite applications is particularly acute when it comes to connectors and cable assemblies, which are some of the bulkier individual elements of an electronic circuit (and, therefore are expected to meet stringent size and weight criteria). With engineers increasingly seeking 'off-the-shelf' interconnect technologies for satellite design, it's important to understand what criteria need to be considered when reviewing datasheets or talking to the connector manufacturer.

Potential applications

The absence of atmosphere and operation in a vacuum presents satellite designers with problems that their counterparts working on earth-based designs often don't have to consider. Consider the high-energy charged X-rays and gamma rays that are produced in space. Because these particles can cause degradation or failure of electronic systems, it becomes essential to choose or develop solutions for shielding against cosmic radiation. This is likely to mean conductive enclosures that prevent the reception of radiation, as well as shielded cables that minimize the impact of radiation on the system.



Jessica Knight,
VP of Sales, Americas, **Harwin**

Cosmic rays are not the only radiation of concern. The effect of thermal radiation when a satellite is in direct sunlight should also be considered, as should thermal cycling that occurs when satellites rotate, placing any electronics on or near the outside in alternating conditions of extreme heat and extreme cold. Indeed, moving between facing the sun and facing the earth, a satellite can experience temperature variations of more than 400°C. This makes assessment of maximum and minimum temperature ratings of the chosen connectors and cabling vital and, in some cases, may mean speaking to suppliers to specify additional testing that anticipates operational life in temperature extremes.

Another issue of concern is outgassing. Also known as offgassing, this is a situation in which the absence of an atmosphere causes plastics and other materials used in connectors and cable assemblies to slowly release volatile compounds as a gas

or vapor that can subsequently impact equipment operation. In the past, this problem has led to degraded performance of charge-coupled-device (CCD) sensors in space probes and impacted camera performance when the released gases condense on other system components such as camera lenses, impacting their performance or making them unusable. Thus, it is important to check maximum levels of outgassing when choosing connectors and cables.

One fundamental aspect to consider when selecting a connector for satellite applications is that of reliability, ensuring that the technology can not only withstand the rigors of lift-off but will also operate as expected for many years without any possibility of 'in-field' repair. This means carefully reviewing connector specifications with respect to their ability to withstand acceleration, shock, and vibration, and adding additional mounts or latches as appropriate.

Finally, so-called SWaP-C pressures mean minimizing size and weight is a challenge for designers of both earth-bound and space-based applications. SWaP-C's significance is particularly important when it comes to satellite applications in which every extra portion of board space and every extra ounce has direct impact on cost. This means it can pay dividends to spend time identifying the smallest and lightest connector solutions for a given performance and reliability rating.

Commercial solutions

The good news is that there is a growing market of commercial interconnect technologies that are not just suitable for many aspects of satellite deployment but, increasingly, have been specifically designed with that target market in mind, being optimized in terms of performance and cost while meeting all the criteria necessary for successful operation in space.

It is now possible, for instance, to find COTS (commercial off-the-shelf) high-reliability 2A and 3A, 2mm and 1.25mm pitch connectors in single- and double-row configurations that are rated for vibration up to 20G and shock up to 100G, and that can withstand temperatures as low as –65°C and as high as +150°C.

Available with jackscrews, stainless steel mate-before-lock screw fixings, or miniature latching for full vibration resistance and maximum strain relief, these connectors conform to rigorous NASA specifications for outgassing and provide a low-profile, low-weight solution for all variations of satellite cable-to-board, board-to-board, and cable-to-cable interconnect requirements. As a result, they are being deployed in applications such as field emission electric propulsion (FEEP) thruster modules that require precise, low-noise handling over the full throttle range as well as attitude control systems, tracking and telemetry, and on-board computing.

Similarly, when it comes to high-power applications such as power control systems and servos, there are a growing number of robust options for satellite designers to choose from. State-of-the-art solutions include compact, high-reliability 8.5mm pitch connectors designed to operate at temperatures from –65°C to +150°C that are provided in shrouded housings, are capable of handling currents up to 60A and voltages as high as 3,000V, and withstanding vibrations and shock of 20G and 100G, respectively.

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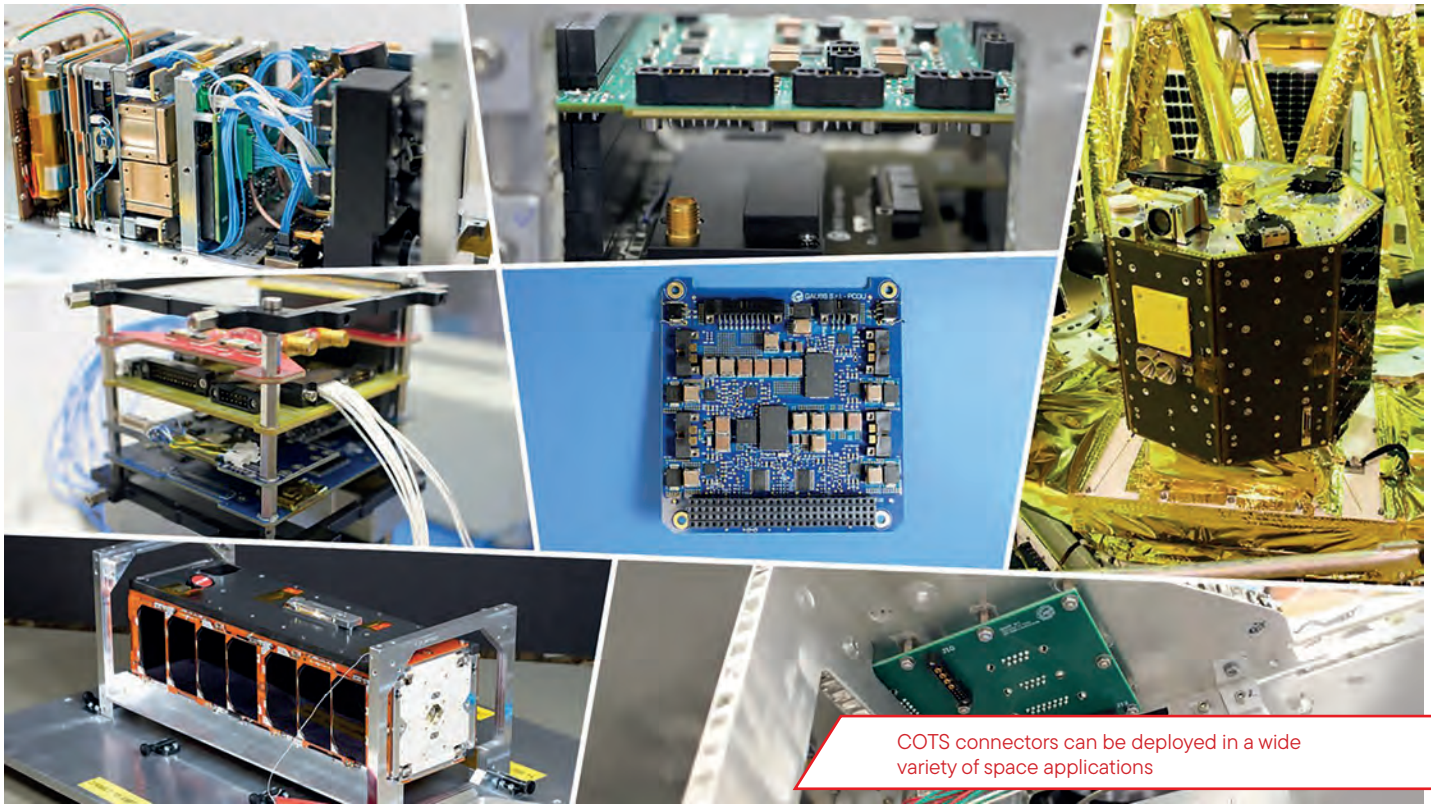

COTS connectors can be deployed in a wide variety of space applications

Enabling the software-defined vehicle

Avijit Sinha, Chief Product Officer, **Wind River**

Three fundamental changes are driving the software-defined vehicle

The automotive industry is experiencing a seismic shift with the advent of software-defined *everything*. This revolution is driven by the growing complexity of developing, integrating, and managing multiple software systems in vehicles. This opens the door for innovation, collaboration, and profitability, not just for the original equipment manufacturer (OEM), but for the entire ecosystem of players who will bring it all together. As we move toward an even more connected and autonomous future, designing a vehicle is about creating quality experiences and customer-desired outcomes, and software is at the epicenter of enabling this reality.

The need for software expertise

The rise of megatrends in connectivity, electrification, autonomy, and shared mobility is pushing automakers to prioritize connected features, infotainment, digital services, and over-the-air software updates as integral parts of the vehicle ownership experience.

Software innovation will be at the heart of this transformation, and building software expertise becomes a crucial need for automotive OEMs and other ecosystem players.

Enabling the SDV

Looking ahead, much of the transformation and consumer value will hinge on software innovation by virtue of software-defined vehicles (SDVs). Automotive companies will increasingly need control over software so that they can improve the vehicle over time and provide differentiated features while reducing time-to-market, decreasing engineering costs, and improving the quality of the software in the vehicle over its lifecycle.

The development, deployment, operation, and servicing of mission-critical intelligent systems will be key for auto manufacturers. Software and tools that support safety-critical applications requiring real-time, deterministic performance will allow auto manufacturers to address a mixed-criticality environment as the industry builds and maintains the software systems of next-generation connected vehicles across the lifecycle. As the industry builds its software expertise, a key need will be to enable a cloud-native edge-to-cloud software platform.

Fundamental changes

Automotive OEMs have been building function-specific electronic control units (ECUs) and function-specific software for years. Typically, they have had big teams and multiple suppliers per program or vehicle platform to cover vehicle software for braking, steering, windshield wipers, automatic windows, and infotainment systems. Automotive companies have been building and integrating software for a long time.

What is new is the agile way of developing software, developing it in the cloud at cloud speed, and then deploying it into the vehicle in real time over the air. Additionally, three fundamental changes are currently driving the software-defined vehicle: in-vehicle architecture, the move from function-specific ECUs to centralized compute, and cloud-driven development with over-the-air updates.

Supporting the software-defined era

In the past, automotive OEMs and their suppliers had teams of hundreds of software engineers working on software projects. Going forward, they're building teams of thousands of software engineers. They are investing billions of dollars towards hiring these software engineers and building the infrastructure required to support the software development and operations effort.

The challenge, when you look at the development tools required for those thousands of engineers, is to determine how they will collaborate, how they will build software, how they will bring it together. That is going to be enormously difficult.

Automotive OEMs will need tools to make those thousands of engineers work well together and work faster to get their software to market. The industry will need software that allows those engineers to be collaborative and productive.

Trusted partners

Some OEMs are building software competency, capability, and platforms themselves. However, the software-defined automobile is complex and has many aspects to consider—hardware, platform, applications, services. Given increasingly software complexity, OEMs should also look to the ecosystem for trusted software partners who have proven expertise and products built using modern cloud-native technologies that can help them accelerate their development and build out the vision of their software journey.

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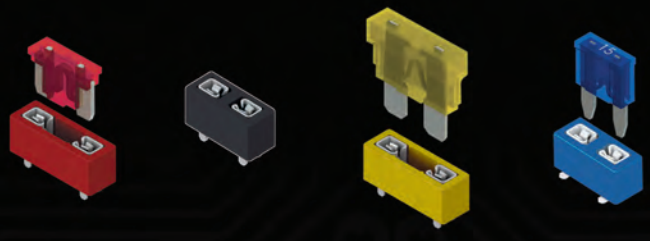
EVs and AVs will continue to develop new electronic devices and equipment, both under the hood and inside the compartment, to make these vehicles more in line with gas powered cars. Doing so will be necessary for long term commercial success.



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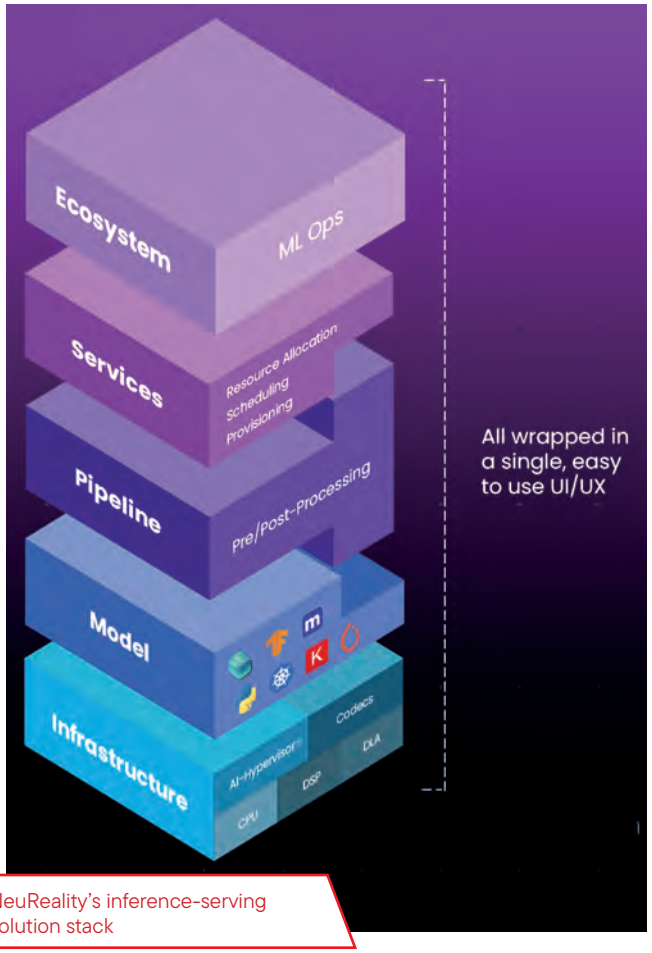
Making AI easy for software developers

by Moshe Tanach, CEO & Co-Founder, **NeuReality**

A solution for more affordable, faster, and scalable AI deployment

In the world of artificial intelligence (AI), every software developer is working on the next big thing—designing, implementing, and testing new deep learning models and AI applications. They have trained AI models to write content creation tools, create chatbots, support data analytics, enhance risk modeling, improve financial forecasting, and tighten cybersecurity—all contributing to commercial productivity. Even before the ChatGPT love affair, the problems did not rest so much with AI training as with AI inference, meaning the costly and complex deployment of trained AI models into real-world applications.



NeuReality's inference-serving solution stack

The tech industry must turn its attention to AI inference, which is the critical second phase of AI. It's not only about developing more accessible affordable AI-centric hardware infrastructure to prop-up AI Inference, but also the software development kits and well-architected application programming interfaces (APIs) that make it easier for software developers to install and use trained AI models. The role of software optimization in AI inferencing cannot be overstated.

Making AI accessible by making it affordable

AI inference has long been a blind spot. The daily costs of AI inference associated with ChatGPT—with reports of one million dollars and higher daily—have pricked the ears of both the tech and non-tech market sectors.

NeuReality anticipated this problem years ago. Although CPUs have helped manage complex AI workflows, they were never designed to host the most advanced deep learning accelerators (DLAs) deployed in three main types of microchips: graphic processing units (GPUs), application-specific integrated circuits (ASICs), and field-programmable gate arrays (FPGAs).

CPU-centric data centers and system architecture are unsuitable when attempting to process extensive amounts of information in the milliseconds required for real-time AI. Moreover, the high cost per AI query makes it impossible for many use cases to deploy and for entire market sectors to participate in the AI age. Our mission at NeuReality was to design an entirely different system architecture to enable a truly AI-centric data center that is accessible to all.

A CPU-centric architecture is akin to a car that can only run as fast as its engine will allow. If the engine in a smaller car is replaced with one from a sports car, the smaller car will fall apart from the speed and acceleration the stronger engine is exerting.

The same applies to a CPU-led AI inference system. A DLA motoring at breakneck speed completing thousands of inference tasks per second will not achieve its full capability with a limited CPU reducing its input and output. Even when an accelerator covers the heavy lifting of a deep learning model processing task, CPUs saturate and reach the peak of their capabilities when processing millions of identical instructions. Ultimately, this bottleneck makes the investment in high-end DLAs a waste.

A complete software stack

AI creation usually comes with quite a bit of trial and error. Software developers must deal with various solution layers, investing their time in deploying the AI-model on high-end DLAs and optimizing the complete pipeline embedding this model. On top of that, developers must focus on data movement and preparation to feed that model's inputs as well as integrate and wrap it with a service layer that allows remote clients to connect and consume the service. Lastly, in order to become citizens in modern data centers, those servers must integrate with existing orchestration and provisioning layers to support large-scale, dynamic AI deployment with high availability.

In designing AI inference of the future, NeuReality's priority has always been to ensure it is accessible, available, and affordable to all, because this is what businesses large and small need to be commercially viable, especially outside the tech industry. This means architecting a complete solution inclusive of robust software tools and inclusive APIs to deploy any trained AI model in any development environment, to connect any AI workflow to any environment, and to offload the complete AI pipeline with tools covering orchestration, provisioning, and runtime.

With an AI service built using this holistic approach, the tech industry can now seamlessly integrate more powerful, affordable, and energy-efficient AI Inference solutions into scientific and commercial data centers—and fully support the growing desire and demand for large language models (LLMs), computer vision models, recommendation engines, financial risk modeling, conversational and generative AI, and beyond. Making AI easy.

Boosting AI inference performance

At NeuReality, we recently launched the NR1 AI Inference Solution, which diverges significantly from conventional servers by harnessing embedded networking, heterogeneous computing, and hardware-based AI pipeline hypervision. Our inference solution stack—with three software layers focusing on model processing, pipeline processing, and services—transforms the overall AI experience while streamlining and enhancing the deployment process for developers, users, and DevOps and IT personnel.

In developing AI pipelines with our software development kit (SDK), developers are given significant flexibility. They can choose to use it as a part of the platform, similar to how NVIDIA MIG works to allocate a part of a GPU, for example. Alternatively, they can exploit pre-made setups, called compute graphs (CGs), in various AI applications to provide the system with more diversity in how that service can be deployed optimally across available accelerator resources. This agility allows developers to deploy the most advanced and complex pipelines more easily, based on the specific needs of their projects.

Through the introduction of our innovative AI Inference Solution, NeuReality has seen performance increase ten-fold and cost savings of up to 90% on AI operations per dollar. It's a dramatic paradigm shift versus incremental improvements to the world's data centers. And with the novel Network Addressable Processing Unit (NAPU), this complete hardware and software solution has dramatically lowered total cost of ownership. As a result, we are on the right path to democratizing AI for all businesses and government entities large and small, including the most recent generative AI and large language models that currently impede business profitability.

Join the Democratization of AI

Today's businesses are already struggling to run commonplace AI applications affordably—from voice recognition systems and recommendation engines to computer vision and risk management—with generative AI's widespread penetration blocked by that financial struggle.

AI requires an entirely new AI-centric design ideal for inferencing: a solution that keeps up with the deluge of requests asked of it, performs optimally while not costing the earth, and—most importantly—becomes a reliable, collaborative tool for software developers rather than one more burden to navigate. By doing so, we can help unleash the next great human achievement together, whether it's combating diseases, enhancing public safety, or creating exciting new software opportunities for the AI job market.

www.neureality.ai

NeuReality NR1 Inference Module

The only constant in life is change

Clive "Max" Maxfield, Editor at **DENA,** CTO of **LogiSwitch,** and freelance technical writer and consultant

I've seen things you people wouldn't believe

The ancient Greek philosopher Heraclitus is credited with saying: "The only constant in life is change." I'm also reminded of my favorite science fiction soliloquy, which was given by the replicant Roy Batty towards the end of the 1982 movie *Blade Runner*. I can hear this in my head as I pen these words: "I've seen things you people wouldn't believe… attack ships on fire off the shoulder of Orion… I watched C-Beams glitter in the dark near the Tannhauser Gate […]" I can't but agree with these sentiments because I've seen things—in the form of technological evolutions and innovations—that even I didn't believe.

When I'm talking to younger folks in general, if I tell them about the technologies that were around when I was a kid, it sounds to them as though I lived in ancient times. Even when talking to young engineers about the tools and technologies that were available when I commenced my career, they look at me as though I was making things up.

Take television, for example. When I was a kid circa the early 1960s, we had one huge set with a small screen. This was cathode-ray-tube (CRT)-based and it weighed a ton. We didn't own it. My parents rented it. If it broke down, a TV repair man came round to the house and fixed it. The picture was presented in glorious black-and-white. The

thought of a color television never even struck me until I saw one in a department store window when I was about six years old. I remember standing in the street with my nose pressed against the glass staring in disbelief. I even remember the program it was showing.

There were only two TV channels in England at that time, and these were only on for part of the day. Children's programs started at 4:00. The news was at 6:00, after which the adults got to watch their programs until broadcasting ceased around 10:00pm (by which time I was in bed). The thought of having high-definition, flat-panel, color televisions in almost every room in the house was beyond our wildest dreams at that time, yet here we are.

And then there were the telephones. We had one black rotary dial phone, wired to the wall, sitting on a corner table at the end of the hall. Also on the table was a 2"-thick telephone directory listing the numbers of all the people in our city. My dad had one sister who lived round the corner from us and two more who had emigrated with their families to Canada. A few weeks before Christmas, my aunt would come to our house, and then she and my mother would attempt to call Canada. First, they would call the local operator, who would connect them with the international operator in London, who would connect them to the international operator in Canada, who would connect them with the local operator in Edmonton, who… nuff said. Now, my mother can contact me 24/7 on my smartphone and we FaceTime for a few minutes every day.

The funny thing is that humans tend to think the technology we see around us is as good as it's going to get. As the distinguished Roman aristocrat Sextus Julius Frontinus famously said in 98AD, "Inventions have long-since reached their limit and I see no hope for further development." He wasn't alone, in 1888, the Canadian-American Astronomer Simon Newcomb opined: "There is little left in the heavens to discover." More than three decades passed before Edwin Hubble showed there were other galaxies beyond the Milky Way. And then there's the American Physicist Albert Michelson who proclaimed in 1894, "The most important fundamental laws and facts of physical science have all been discovered." Imagine his face when Joseph John Thomson discovered the electron three years later.

It's not all that long ago that things like tablet computers, smartphones, GPS, and connected devices were the stuff of dreams. Now we take them for granted and think nothing of them. Many people believe that we've got as far as we're going to go. All I can say is, "The only constant in life is change!"

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AI for PCB layout design: a new frontier in productivity and collaboration

Bob Potock, VP Marketing,
Zuken USA

AI introduces exciting new opportunities for productivity and collaboration in the mature discipline of PCB layout design

Integrating artificial intelligence (AI) into various processes has become a transformative force in the rapidly evolving electronics and electrical engineering field. Within the hardware design process, PCB layout design, a pivotal facet of electronic product development, is experiencing a significant shift with the infusion of AI. Let's dig into AI for PCB layout design to explore its profound impact on efficiency gains, its limitations, and its role as a collaborative tool.

Hardware design productivity

The digital age ushered in a wave of technological advancements, and AI's role in hardware design is proving to be a game-changer.

Historically, PCB layout designers grappled with their craft's repetitive activities, like component placement, trace routing, and design rule checks. These essential tasks can be both labor-intensive and mentally taxing.

We can teach AI tools to handle these repetitive tasks. An AI tool developed specifically for PCB layout can swiftly process and analyze vast amounts of data, making optimal choices for component placement, signal routing, power distribution, and thermal management. Based on machine learning from existing successful place and route projects, the AI-generated boards will mirror past human-created PCB designs better than a traditional autorouter. While a conventional autorouter is based on algorithms, the AI-based routing engine can learn from design examples.

One of the most immediate benefits of incorporating AI into hardware design is its ability to handle complex tasks. A good example is asking an AI copilot (i.e., an AI-based utility) to optimize the BOM (bill of materials) for cost. The AI copilot can search the supply chain for equivalent and more cost-effective components. BOM optimization is a complex manual task that AI can take over and address in seconds or minutes.

The implications of this shift are profound. AI-driven automation accelerates and efficiently manages component placement, optimizing signal integrity, power distribution, and thermal management. The result? Faster time-to-market without compromising quality or functionality. In today's fast-paced electronics industry, this acceleration is invaluable.

Training with high-quality designs

AI machine learning is essentially transferring design strategies to your next project. Companies produce various electronic products utilizing different technologies and implementation strategies. The AI engine needs to be trained on each design type and strategy. Each company or department can produce an AI tool tuned for their products and technology. Even within your company, each department can train the AI engine for their specific needs. The ability to transfer or preserve design knowledge specific to a product is a powerful concept.

Boards can contain a variety of different technologies. Consider company A, which uses DDR4 or DDR5 memory on all its boards. Company B builds communication hardware and utilizes SERDES with high pin-count FPGAs. Routing these boards requires specialized knowledge and experience. The ability to teach and create a "brain" for each technology enables the brain to identify different technologies, each with differing place and route requirements. A company can target different design types by using several trained brains (i.e., AI place and route knowledge). Training the brains with high-quality board designs will produce similar high-quality results going forward. While training with low-quality board designs will produce low-quality results. Choose your designs carefully.

Once the brain learns to place and route your board type, the process involves selecting which brain to apply and then hitting the Go button. With the AI tool as a collaborator, the place and route process is accelerated and delivers high-quality results.

Limitations of artificial intelligence

AI's role in PCB design is not to render designers obsolete but to augment their abilities and assist with their current tasks. It acts as a powerful tool that complements human expertise. Tasks once dominated by manual labor are now executed with less human involvement, freeing designers to focus on other critical tasks.

AI does have limitations. There will be instances when the AI brain can not complete the place and route task (e.g., new technology

with new routing rules). The untrained brain will struggle. The AI brain also requires computational power. A server will be necessary to analyze the board, create, and then execute a plan. For cases where the AI brain can not complete the board, human intervention will be required.

Think of AI as a copilot, ready to be part of a team to complete a specific job.

Reap the benefits

AI-based PCB layout design tools have limitations, but the benefits are clear. The often challenging and time-consuming task of placing and routing a board can be completed faster using AI to deliver human-like results. The AI tool can continually learn, making for a productive copilot. Time previously spent on place and route can be reallocated to explore new solutions and develop new skills.

Once the AI brain has been taught how to place and route a particular type of design, the brain will deliver consistent and predictable results. And it has 24/7 availability to deliver results more quickly.

The human-AI partnership

The integration of AI into PCB design marks the evolution of a collaborative partnership between human intelligence and machine learning capabilities. Think of it as having a highly skilled teammate who excels in specific tasks while complementing your unique strengths.

AI augments the creative and problem-solving abilities of PCB designers. It provides the precision and speed required for optimizing design layouts, managing complex components, and ensuring compliance with industry standards. This collaboration results in more innovative and efficient PCB designs.

Designing PCBs is both an art and a science. With its analytical prowess, AI enhances productivity by completing complex tasks with human-like results. This, in turn, allows designers to focus on creating innovative, functional, and aesthetically pleasing electronic products that get to market faster.

Embracing the future of PCB design

As we embrace the AI revolution, it's essential to dispel the notion that AI threatens PCB industry job security. Instead, it should be viewed as a catalyst for growth and innovation in the industry. PCB designers can look forward to a future where AI enhances their roles, drives efficiency, and contributes to creating cutting-edge electronic products.

AI is not just a buzzword; it's a valuable design ally, working hand-in-hand with PCB designers to unlock new possibilities and shape the industry's future. By upskilling and embracing this technology, designers can confidently navigate the evolving landscape, knowing that AI is here to assist, not replace. The synergy between human ingenuity and AI capabilities is key to unlocking the full potential of PCB design.

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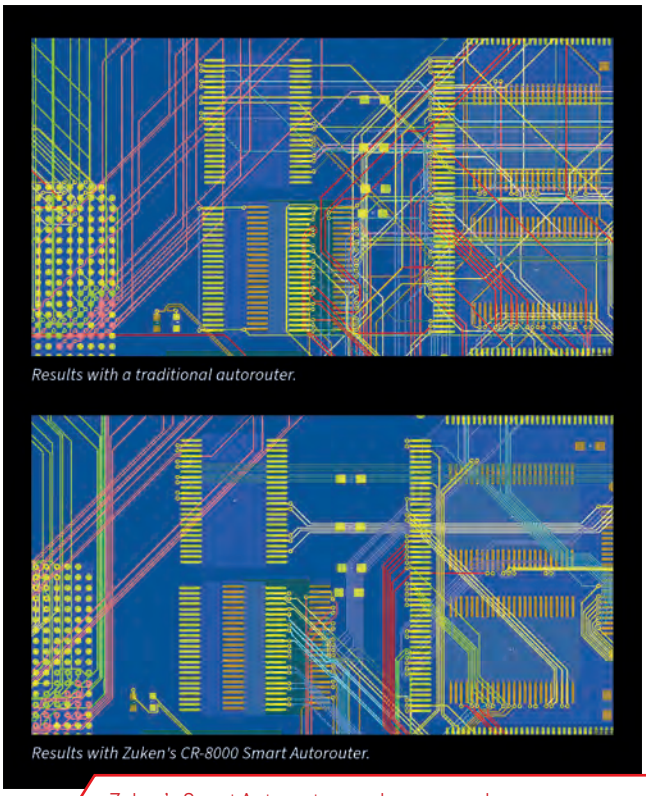
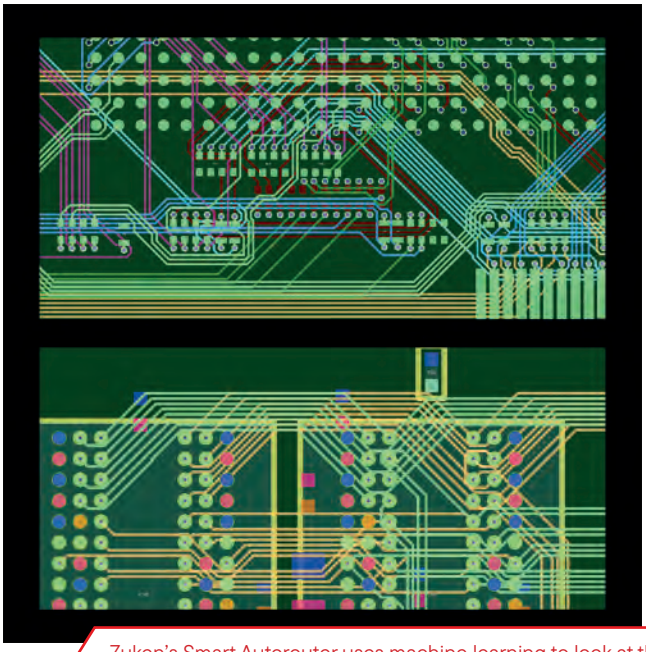


Zuken's Smart Autorouter produces more human-like results compared to a traditional autorouter



Zuken's Smart Autorouter uses machine learning to look at the board holistically and apply what it has learned to the design

A solution to knock down the memory wall

Lauro Rizzatti, Business Advisor to **VSORA**

After dominating the computing landscape since the mid-1940s, the CPU architecture got demoted. As long as the escalating demand for powerful data processing outpaced the requirements for high bandwidth data movement, CPUs delivered what was expected from them. The rise of big data feeding high-performance computing (HPC) tilted the balance in favor of massive data movement throughput. A case in point is the elaboration of transformer algorithms in generative AI (GenAI) models that requires moving hundreds of billions of bytes every clock cycle, a daunting task that the CPU architecture cannot perform.

Never sitting idle, the semiconductor industry has been at work devising a multitude of alternative solutions, some more effective than others.

GPUs, FPGAs. and ASICs replaced CPUs in data centers and AI applications. However, while they boost data processing performance, none improves data movement throughput.

The culprit is the memory—specifically, inadequate memory bandwidth that has not kept up with the progress in data processing. The ensuant gap, which is known as the "memory wall," hinders the efficiency of any processors. It also dramatically increases power consumption and thwarts their scalability.

The inherent potential of AI (specifically, GenAI) is severely incumbered by the limited bandwidth of memories. Although GPUs are the choice for AI learning in data centers, their efficiencies reportedly hover in a range of a single digit (that's 1% to 9%).

One approach to address the memory wall, refined over the years, and still widely adopted, consists of buffering the memory channel in the proximity of the processor by inserting a multi-level hierarchical cache. By caching frequently used data, datapaths drastically shrink.

Moving down the hierarchy from the processors, the storage fabric changes from individual-bit addressable registers to tightly coupled memory (TCM), scratchpad memory, and cache memory. While storage capacity increases, speed of execution drops since more and more cycles are required to move data in and out of the memory.

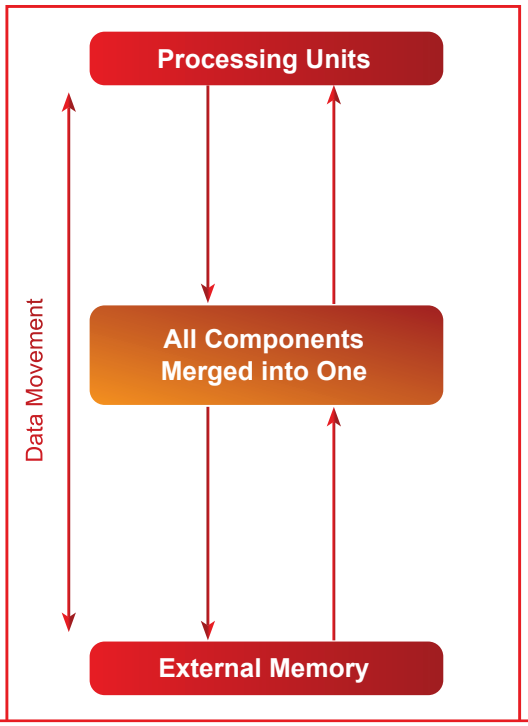
In an ideal scenario, replacing TCM, scratchpad, and cache with registers would lead to a massive speed up. That is what French startup VSORA did. The VSORA approach collapses the hierarchical memory structure into a large high bandwidth tightly coupled memory accessed in one clock cycle.

To the processor, the VSORA TCM looks and acts like a sea of registers in the amount of MBytes vs. kBytes in conventional computing architectures. The ability to access any memory cell in one clock cycle yields high execution speed, low latency, and low-power consumption. It also requires less silicon area. Loading new data from external memory into the TCM while the current data is processed does not affect system throughput.

This architecture allows for high utilization of the processors even when elaborating challenging applications. Typically, the efficiencies in executing large transformer models such as ChartGPT-4 on cutting-edge GenAI processors drop to single digits percentage. Instead, the VSORA approach on the same workload yields efficiencies in excess of 50%.

VSORA's memory approach could reach two orders of magnitude higher processing efficiencies. That would lower the annual cost to run 100,000 queries per second—the standard established by Google search—on a GPT-4 system from hundreds of billions of dollars to fewer than $10 billion.

www.vsora.com



VSORA's approach collapses the multi-level hierarchical cache structure into one level accessible in one clock cycle

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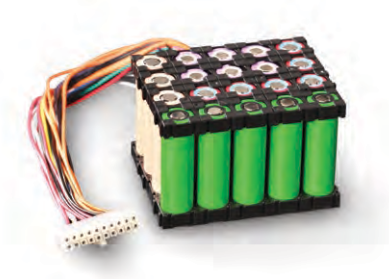

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